Fraunhofer
CNT

FRAUNHOFER CENTER NANOELECTRONIC TECHNOLOGIES

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2010

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PREFACE

Das Fraunhofer Center Nanoelektronische Technologien (CNT) kann auf ein erfolgreiches Jahr 2010 zurückblicken. Erste Schritte einer Neuausrichtung, die durch die Insolvenz des Industriepartners Qimonda im Jahr 2009 notwendig geworden waren, konnten 2010 erfolgreich umgesetzt werden. Dazu beigetragen hat auch der wirtschaftliche Aufschwung nach der Krise im Jahr 2009 in der Mikroelektronik, verbunden mit Aufträgen auch von mittelständischen Unternehmen. Einmal mehr erwies sich dabei, dass die Ergebnisse aus der Nanoelektronik zunehmend Anwendungen auch in Systemen der Mikroelektronik finden – „Nano for Micro".

2010 was a successful year for Fraunhofer Center Nanoelectronic Technologies (CNT). First steps towards the realignment, which became necessary due to the insolvency of the business partner Qimonda in 2009, were taken successfully. The economic revival after the crisis of the microelectronic market in 2009 and various orders - as well from medium-sized companies - contributed to these achievements. Once more it was demonstrated that the results from nanoelectronics are used increasingly in microelectronic systems – "nano for micro".

Als beständiger Faktor, nicht nur in den Zeiten der Krise, erwies sich die Kooperation mit unserem Industriepartner GLOBALFOUNDRIES. Wesentliche Beiträge zur Weiterentwicklung der Nanoelektronik konnten durch das Fraunhofer CNT geleistet werden. Wichtige Projekte mit einer Umsetzung von Forschung in Materialien und Prozessen wurden gemeinsam erfolgreich zum Abschluss gebracht und neue Forschungsinhalte definiert. Mehrere Projekte und Vereinbarungen mit anderen IC-Herstellern und Anlagenherstellern sowohl im Bereich Abscheidung und Hoch-Temperatur-Behandlung, als auch bei Testsystemen erweitern das Kompetenzspektrum.

The cooperation with our industrial partner GLOBALFOUNDRIES proved to be a constant factor, not only in times of crisis. Fraunhofer CNT provided essential contributions for the further development of the nanoelectronic. Several important projects with our partner were completed successfully by implementing research results related to materials and processes. Besides, new research subjects were defined. Furthermore, several projects and agreements could be obtained with other IC and equipment manufacturers in the field of deposition, high-temperature treatment and test systems.

Diese Aktivitäten und die Unterstützung durch öffentlich geförderte Projekte ermöglichten eine Stabilisierung und einen Kompetenzaufbau im Fraunhofer CNT.
Beispielhaft sei hier das vom BMBF geförderte Projekt BRIDGE genannt, das 2010 erfolgreich abgeschlossen wurde. Fachgebietsübergreifend wurde es in den Bereichen Strukturierung und Abscheidung durchgeführt.

These activities and the support by publicly financed projects enabled the stabilization and the development of competences at Fraunhofer CNT. BRIDGE is one example of a project, which was financed by BMBF and which could be completed successfully in 2010. Our competences in the field of structuring and deposition contributed to the success of this project.

Director: Prof. Dr. Peter Kücher

Die im Fraunhofer CNT vorhandenen Kompetenzen können so unter anderem für eine Anwendung von MIM-Strukturen in mikroelektronischen Systemen weiterentwickelt werden.

Mit dem energieautarken Sensorsystem, von Wissenschaftlern des Kompetenzbereiches Devices & Integration entwickelt, stellt das Fraunhofer CNT erstmalig seine Prozesse in einer Systemanwendung dar.

Durch die vom Freistaat Sachsen geförderten Aktivitäten im Bereich Elektronenstrahllithographie wurde die herausragende Qualität und das Potential dieser Technologie gerade in der breiten Anwendung für die Mikrosystemtechnik und Nanoelektronik bei Strukturen unter 30 nm demonstriert.

Diese nur beispielhaft genannten Projekte haben dazu beitragen, Innovationen in den sogenannten „Key Enabling Technologies" in der EU (COM (2009) 512/3) voranzutreiben. Damit liefert das Fraunhofer CNT auch weiterhin einen wichtigen Beitrag für die herausragende Stellung Dresdens als Mikroelektronik-Standort.

Besonders nennenswert ist der erfolgreiche Abschluss der ersten Doktoranden am Fraunhofer CNT. Dadurch zeigte sich auch die Effektivität mit der die Arbeiten, gerade durch die enge Zusammenarbeit mit der Industrie und den betreuenden Professoren, durchgeführt werden konnten.

The existing competences at Fraunhofer CNT can continuously be refined, e. g. for the application of MIM structures in microelectronic systems.

Due to this energy self-sufficient sensor system, which was developed by scientists of the Devices & Integration group, Fraunhofer CNT could demonstrate its processes in a system application for the first time.

Owing to the extensive research activities in the field of electron beam lithography, which were supported by the Free State of Saxony, the outstanding quality and the potential of this technology could be shown. This technology offers a broad range of application possibilities, especially for the microsystems technology and nanoelectronics with structures below/less than 30 nm.

These exemplarily mentioned projects contributed to further development of innovations within the so-called „Key Enabling Technologies" in the EU (COM (2009) 512/3). Thus Fraunhofer CNT continues to make an important contribution to Dresden's outstanding position as a location for microelectronics.

Furthermore, I was especially pleased about the successful graduation of the first Ph.D. students at Fraunhofer CNT. Thus the effectiveness of the close cooperation between industry and the supervising professors was demonstrated successfully.

PREFACE

Am 28. Oktober 2010 fand der erste „Fraunhofer CNT Research Day“ statt. Wir konnten mehrere Experten führender Unternehmen (z. B. IBM, GLOBALFOUNDRIES, ASM, Applied Materials) begrüßen, die neben Wissenschaftlern aus unserem Institut neueste Erkenntnisse und Strategien aus verschiedenen Fachgebieten vorstellten. Knapp 100 Teilnehmer und das positive Feedback der Gäste lassen uns auf eine gelungene Veranstaltung zurückblicken.

Einen weiteren Meilenstein stellt die Gründung des ALD Lab Dresden in Zusammenarbeit mit der TU Dresden dar. Es ermöglicht die Zusammenführung von Kompetenzen auf dem Gebiet der Atomlagenabscheidung (ALD) am Standort Dresden. Die bereits seit fünf Jahren bestehende Zusammenarbeit erhielt nun mit der Dachorganisation „ALD Lab Dresden“ einen offiziellen Rahmen.

Das Fraunhofer CNT ist mit seinen Kompetenzbereichen und seiner Ausrichtung neu aufgestellt. Für das Jahr 2011 und darüber hinaus ermöglicht dies ein weiteres Wachstum und lässt uns positiv in die Zukunft blicken. Dies verdanken wir unseren engagierten und kompetenten Mitarbeitern und in erster Linie unseren Partnern und Förderern, denen ich an dieser Stelle besonders für das entgegengebrachte Vertrauen danken möchte.

Prof. Dr. Peter Kücher

The first „Fraunhofer CNT Research Day” took place on 28th October 2010. Renowned experts of leading companies of the microelectronics industry, such as IBM, GLOBALFOUNDRIES, ASM and Applied Materials, as well as scientific staff representatives of Fraunhofer CNT gave exciting talks on their latest research results, strategies and innovations. The large number of participants and the positive feedback show the success of the Research Day.

The foundation of the ALD Lab Dresden in cooperation with the Dresden University of Technology set another milestone. Thus, the existing competences in the field of atomic layer deposition (ALD) can be combined in an optimal way. With the foundation of the „ALD Lab Dresden”, an official framework was finally formed for this cooperation, which has already existed for five years.

With its competence areas and its new strategic focus, Fraunhofer CNT realigned its positioning. This enables a further growth in 2011 and beyond and gives a positive outlook on the future. I would like to use this opportunity to thank our highly motivated and competent employees and above all our business partners and supporters for their confidence.

Prof. Dr. Peter Kücher

FRAUNHOFER CNT IN PROFILE

Forschung und Entwicklung im Fraunhofer CNT

Das Geschäftsfeld des Fraunhofer CNT umfasst die Entwicklung von Prozessschritten und Materialien sowie die physikalische und elektrische Charakterisierung für High-Performance-Logik, Derivate (z. B. embedded DRAM) und Speichertechnologien für flüchtige und nicht-flüchtige Bauelemente.
Zielsetzung der Einrichtung ist es, innovative Einzelprozesslösungen für nanoelektronische Systeme vor allem auf 300 mm Wafern mit Industriepartnern und anderen Forschungseinrichtungen so zu entwickeln, dass diese schnell in ein industrielles Fertigungsumfeld übertragen werden können.

Das Leistungsangebot des Fraunhofer CNT gliedert sich in fünf Kompetenzbereiche:

- Analytik
- Funktionale Elektronische Materialien - Front End of Line
- Funktionale Elektronische Materialien - Back End of Line
- Devices & Integration
- Strukturierung

Die Kompetenzbereiche forschen vor allem auf folgenden Gebieten:

- Leading Edge Technologie für die Nanoelektronik
- Technologieentwicklung, basierend auf 300 mm Wafern in enger Verbindung und der Anwendung an eine Volumenfertigung
- Nano-Mikro-Integration
- Nano-Analytik und Metrologie

Research and Development at Fraunhofer CNT

The business areas of Fraunhofer CNT include the development of processes and materials as well as the physical and electrical characterization of high-performance-logics, derivates (e. g. embedded DRAM) and memory technologies for volatile and non-volatile devices.
In close cooperation with industrial partners and other R&D organizations, the objective of our institute is to develop innovative unit process solutions for nanoelectronic systems on 300 mm silicon wafers. The aim is to transfer research results fast into industrial manufacturing.

The range of services offered by Fraunhofer CNT is divided into five competence areas:

- Analytics
- Functional Electronic Materials - Front End of Line
- Functional Electronic Materials - Back End of Line
- Devices & Integration
- Patterning

The competence areas do research especially in the following fields:

- Leading edge technology for nano electronic
- Development of technology based on 300 mm wafers in close connection and application of manufacturing
- Nano-micro-integration
- Nano analytics and metrology

Ausstattung

Für das Fraunhofer CNT stehen derzeit 800 m² Reinraumfläche (Reinraumklasse 1000) sowie eine Infrastruktur zur Verfügung, die dem Industriestandard entspricht. Zusätzlich zu den ca. 40 Anlagen im Reinraum können umfangreiche Analyse- und Metrologieverfahren für die Forschung und Entwicklung sowie die Bausteincharakterisierung genutzt werden.
Die Einrichtung unterhält keine durchgängige Prozesslinie in der alle notwendigen Prozessschritte zur Realisierung höchstintegrierter Chips zur Verfügung stehen. Sie verfügt aber über neue, fertigungstypische Prozessgeräte, an denen die Partner zusammen mit den Wissenschaftlern im Fraunhofer CNT forschen und entwickeln können.

Teilprozessierte Wafer kommen von GLOBALFOUNDRIES - die innovativen Prozessschritte werden im Fraunhofer CNT durchgeführt. Die gewonnenen Erkenntnisse können dann sofort in die praktische Erprobung in der angrenzenden Fertigung übertragen werden. Dadurch lassen sich sowohl Investitionen für die Partner minimieren, als auch ein schnellerer Zeitablauf ermöglichen.

Environment

At present, Fraunhofer CNT uses 800 m² clean room area (class 1000) and an infrastructure which meets industry standards. In addition to 40 clean room tools, scientists at Fraunhofer CNT use considerable analytical and metrological processes for R&D as well as for the characterization of nanoelectronic devices.

The institute does not maintain a continuous process line to cover all the necessary process steps in order to realize high-integrated memory chips. However, Fraunhofer CNT possesses new process tools which are typical of production and enabling common research and development with its partners.

Pre-processed wafers are provided by GLOBALFOUNDRIES – innovative process steps will be operated at Fraunhofer CNT. Thus, the results can be transferred immediately into manufacturing. This enables partners to reduce their capital expenditures. Moreover, it allows a faster schedule.

FRAUNHOFER CNT IN PROFILE

Kooperationspartner in unmittelbarer Umgebung

Das Fraunhofer-Center Nanoelektronische Technologien - 2005 entsprechend dem Modell einer Public-Private-Partnership gegründet - ist neben der erfolgreichen Kooperation mit dem Halbleiterhersteller GLOBALFOUNDRIES Dresden Module One LLC & Co. KG auch für die Zusammenarbeit und Durchführung von Projekten mit verschiedenen Forschungseinrichtungen, Industriepartnern und Universitäten sowie Zulieferfirmen der IC-Industrie wie Material- und Geräteherstellern offen.

In unmittelbarer Umgebung des Fraunhofer CNT befinden sich die Halbleiterhersteller GLOBALFOUNDRIES, Infineon und X-Fab. Dazu bietet Dresden, eingebettet in Silicon Saxony, ausgezeichnete Standortbedingungen für das Fraunhofer CNT als etablierte Forschungsplattform der Nanoelektronik. Durch die lokale Nähe zu den Fertigungslinien des Partners und das vorhandene Know-how können viele Synergieeffekte genutzt werden. Dadurch ist es möglich, Entwicklungen und neue Prozesse schnell in die Fertigungsabläufe einzubauen, was es wiederum erlaubt Herstellungskosten und -zeit zu sparen.

„Durch die Nutzung von Synergien zwischen der Referenz von Fertigungslinien, basierend auf modernster 300 mm Wafertechnologie, sowie dem Fachwissen unserer Mitarbeiter können wir Projekte erfolgreich und zeitnah durchführen."
Prof. Dr. Peter Kücher

Cooperation partner in the immediate vicinity

Fraunhofer Center Nanoelectronic Technologies was founded in 2005 according to the model of a public private partnership. A part from the successful cooperation with the semiconductor manufacturer GLOBALFOUNDRIES Dresden Module One LLC & Co. KG, the institute is open for the collaboration and execution of projects with different research organizations, industrial partners, universities as well as semiconductor suppliers such as material and tool manufacturers.

The semiconductor manufacturers GLOBALFOUNDRIES, Infineon and X-Fab are located close to Fraunhofer CNT. In addition, Dresden and Silicon Saxony offer excellent site conditions. Because of the proximity to the manufacturing lines of the partners and of the established know-how, Fraunhofer CNT benefits from numerous synergy effects. Thus, it is possible to implement innovative developments and new processes fast into manufacturing. It also enables the partners to save time and production costs.

„Benefiting from synergies between the reference of the manufacturing lines on the basis of latest 300 mm wafer technology as well as of the know-how of our employees, we are able to perform our projects successfully and immediately."
Prof. Dr. Peter Kücher

FRAUNHOFER CNT IN FIGURES

Das Fraunhofer CNT erwirtschaftete 2010 einen Ertrag von ca. 9,8 Mio Euro. Der Betriebshaushalt setzte sich zu ca. 23 % aus Wirtschaftserträgen, zu etwa 36 % aus Erträgen aus nationalen öffentlichen Projekten, zu rund 7 % aus EU-Erträgen, zu rund 30 % aus sonstigen Erträgen und nur zu 4 % aus Sonderfinanzierungsmitteln zusammen.

Zur Bearbeitung der Forschungsaufträge stehen auf 800 m² Reinraumfläche und 200 m² Laborfläche modernste Laborausstattungen und Großgeräte zur Verfügung. Der Anlagenpark umfasst Abscheide- und Ätzanlagen für die Wärmebehandlung bei Hochtemperaturen sowie Inspektions- und Analysegeräte zum Bestimmen von Defekten und dem Messen von Schichteigenschaften.

Zum Jahresende 2010 beschäftigte das Fraunhofer CNT 51 festangestellte Mitarbeiter. Das Personal setzte sich aus 34 Wissenschaftlern einschließlich 10 Doktoranden, 7 technischen Mitarbeitern und 10 Mitarbeitern in Management und Verwaltung zusammen. Mit modernstem Anlagenpark, intensiver Vorlaufforschung sowie einer langjährigen Industrieerfahrung stehen die Mitarbeiter des Fraunhofer CNT ihren nationalen und internationalen Kunden und Partnern zur Seite, um Innovationen für die Zukunft nutzbar zu machen.

In 2010 Fraunhofer CNT generated revenues of about 9.8 million Euro. The operation budget was composed of 23 % of industry returns, 36 % earnings from national public projects, 7 % of EU earnings, 30 % of other revenues and only 4 % of special financing.

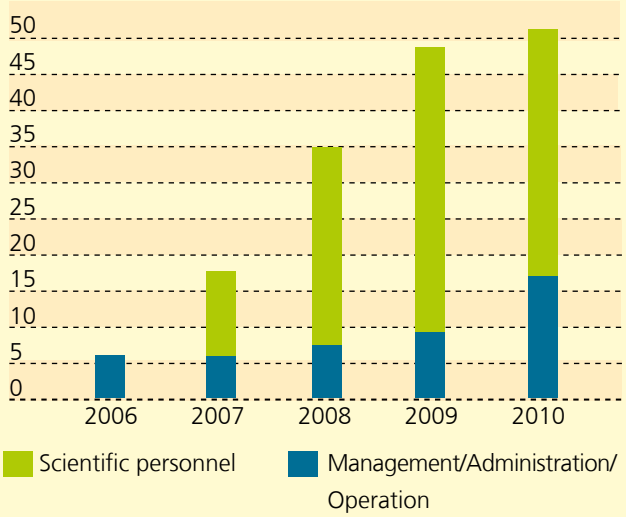
In order to process R&D wafers professionally, Fraunhofer CNT has an area of 800 m² clean room and 200 m² laboratory available which are equipped with the latest semiconductor R&D tools. The equipment ranges from deposition and etching tools used for the heat treatment at high-temperatures as well as from inspection and analytic tools which are used for the characterization of defects and layers.

In the end of 2010, Fraunhofer CNT employed 51 permanent staff. The personnel was composed of 34 scientists including 10 Ph.D. students, 7 technicians and 10 employees in administration and management. Equipped with the latest equipment, intense initial research and a long-lasting industry know-how, employees of Fraunhofer CNT provide support to their national and international customers and partners in order to realize innovations in the future.

Expenditures and Revenues 2010

	in k €	in %
Annual Budget 2010	**9.827**	
Expenditures	**9.827**	
Personnel Expenses	2.639	27,0
Equipment/Clean Room Expenses	5.971	61,0
Other Operating Expenses	1.217	12,0
Revenues	**9.827**	
Industry	2.280	23,0
Publicly (national)	3.555	36,0
Publicly (EU)	682	7,0
Others	2.945	30,0
Additional Income	365	4,0

Personnel 2006 - 2010



Head of Administration: Katja Böttger

Das Fraunhofer CNT hat 2010 ca. 5,5 Mio Euro investiert, um das modernste technische Equipment zu erweitern. Diese Investitionen wurden aus dem Europäischen Fond für Regionale Entwicklung und vom Freistaat Sachsen gefördert.

Aufgrund der beständigen Kooperation mit der GLOBALFOUNDRIES kommt ein Großteil der Finanzierung aus der Industrie. Die öffentlichen Erträge resultieren insbesondere aus einem großen Forschungsprojekt. Thema des vom BMBF geförderten Projekts war die Entwicklung von Basistechnologien für die Umsetzung der ITRS Roadmap. Die Zielstellung des Forschungsprojekts war es, für kritische Einzelprozesse wie **Strukturierung, Ätzung und Abscheidung**, innovative Lösungen für die Produktion von Mikrochips **auf 300 und 200 mm Wafern** bereitzustellen. Ein weiterer Aspekt war die Integration von Einzelprozessen sowie die Weiterentwicklung analytischer Methoden.

Das Fraunhofer CNT war 2010 weiterhin an einem Projekt zur Durchführung von Modellrechnungen zum **chemisch-mechanischen Planarisieren (CMP)** von dielektrischen Materialien bei der Graben- und Zwischenlagenisolation, als Unterauftragnehmer der TU Dresden beteiligt.

In einem Projekt der Namlab gGmbH entwickelte das Fraunhofer CNT **ALD-Abscheidetechniken** für Hafniumdioxid basierende neue Materialien und wenige atomlagendicke Schichtsysteme.

Thema eines weiteren EU-Projektes ist die Weiterentwicklung eines zukunftweisenden, haftstellenbasierten, nichtflüchtigen Speicherkonzeptes. Ziel des Projektkonsortiums, unter Leitung des Halbleiterherstellers Numonyx, ist die **Entwicklung eines Demonstrators auf Basis von Sub-40 nm Prozesstechnologien**.

In 2010, Fraunhofer CNT invested about 5.5 million Euro in order to upgrade its leading edge equipment. These investments have been funded by the European Regional Development Fund (ERDF) of the European Union and by the Free State of Saxony.

Due to the consistent partnership with GLOBALFOUNDRIES the majority of the financing comes from the industry. Public earnings result basically from one broad research project. This project, which was funded by the BMBF, focused on the development of basic technologies in order to implement the ITRS roadmap. The objective of this R&D project was to provide innovative solutions for the production of microchips on the basis of **300 and 200 mm wafers**, especially for critical unit processes such as **patterning, etching and deposition**. Another aspect was the integration of unit processes as well as the further development of analytical methods.

In 2010, Fraunhofer CNT was also involved in a project as a subcontractor of the Dresden University of Technology. The main content of this project was to develop new models for the **chemical-mechanical planarization (CMP)** of dielectric materials used in shallow trench isolation (STI) and interlayer dielectric (ILD).

In a further project, Fraunhofer CNT developed together with the Namlab gGmbH, **ALD processes** for hafniumdioxide based new materials and atomic layer systems.

The topic of another EU-project is the further development of a trendsetting trapping based on non-volatile memory concept. The aim of the project consortium, which is led by the semiconductor manufacturer Numonyx, is **the development of a demonstrator on the basis of sub-40 nm process technologies**.

Entrance of Fraunhofer CNT

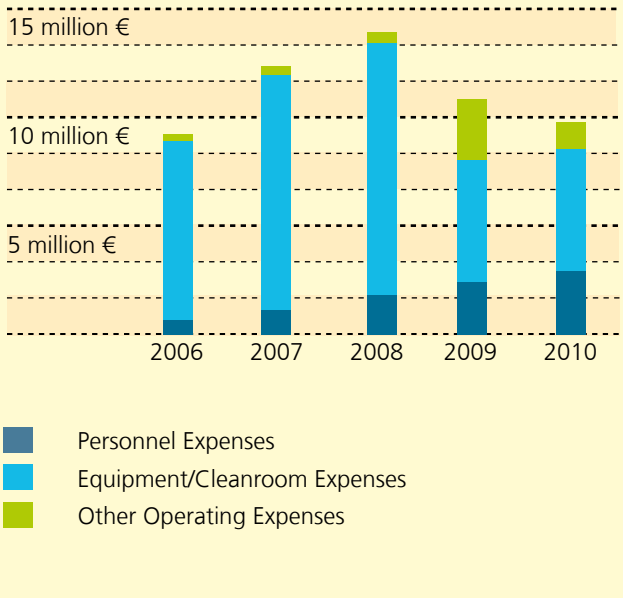
In einem weiteren EU-geförderten Projekt, welches 2010 erfolgreich abgeschlossen werden konnte, wurde die **maskenlose Elektronenstrahllithographie** für die Mikrochipherstellung weiterentwickelt. Dazu wurden zwei unterschiedliche Ansätze für die **E-Beam-Lithographie** mit mehreren parallelen Elektronenstrahlen evaluiert. Das Fraunhofer CNT brachte hier mit seinem Center of Competence E-Beam seine herausragenden Erfahrungen in der maskenlosen Strukturierung kleinster Leiterbahnen ein.

Dank unserer Kooperation mit dem Industriepartner GLOBALFOUNDRIES konnten im Jahr 2010 neue Projekte erfolgreich am Fraunhofer CNT etabliert werden.
Gefördert von der Sächsischen Aufbaubank (SAB) und dem Europäischen Fonds für regionale Entwicklung (EFRE) in Höhe von 3,8 Mio Euro, beschäftigt sich ein neues Projekt mit der **Entwicklung zukünftiger High-k Gate-Dielektrik-Transistoren** einschließlich

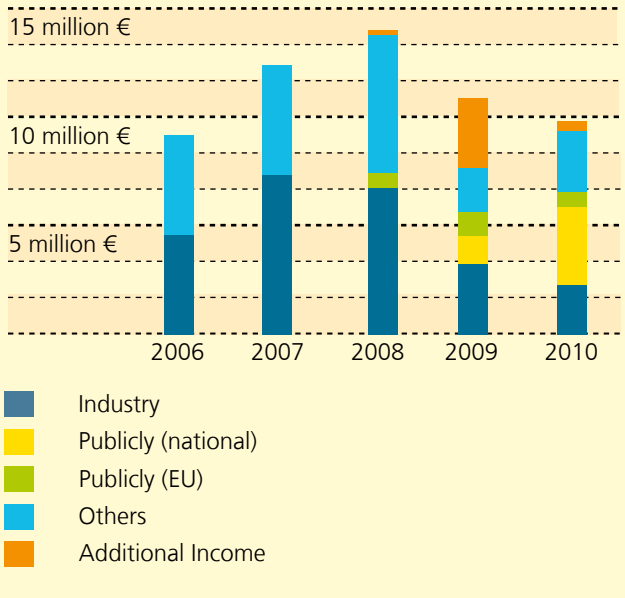
A further EU-financed project was successfully completed in 2010. The scope of this project was to enhance the maskless electron beam lithography for the manufacturing of microchips. Two different approaches with multiple parallel electron beams were evaluated for the E-Beam lithography. In the course of this project the E-Beam center of competence at Fraunhofer CNT contributed its outstanding scientific experiences in the maskless structuring of minimum conductors.

In 2010, new promising projects started at Fraunhofer CNT due to the close cooperation with the industrial partner GLOBALFOUNDRIES.
A new project which is financed by the Sächsische Aufbaubank (SAB) and the European fund for regional development (EFRE) with an amount of 3.8 million Euro focuses on the **development of future high-k gate-dielectric transistors** including a feasibility

Development of Operating Budget 2006 - 2010



Development of Project Revenue 2006 - 2010



einer Machbarkeitsstudie für ferroelektrische Speicher. Gemeinsam mit GLOBALFOUNDRIES arbeiten die Wissenschaftler des Fraunhofer CNT an der **Optimierung von ALD-Prozessen zur Herstellung von High-k-Stapeln**. Ein wichtiger Teil der Forschungsarbeiten beinhaltet auch die **Analyse von high-k/metal Gate Schichten im SRAM mittels der Atomsondentomographie**.

Es wurden weitere Projekte durch GLOBALFOUNDRIES beauftragt, wie die **Entwicklung einer Verdrahtungstechnologie für kleinste Strukturen** unter Berücksichtigung der wachsenden Anforderungen an die elektrische Zuverlässigkeit sowie auch ein Projekt zu Prozessdemonstrationen von dünnen Titannitrid-Schichten mit einem ASM A412 100 Waferbatch-Prozess für Replacementgate.

Zwei weitere Projekte starteten bereits vor 2010. In beiden, von der Sächsischen Aufbaubank (SAB) geförderten Projekten ist das Fraunhofer CNT als Unterauftragnehmer involviert.
Das erste Projekt beschäftigt sich mit der schädigungsfreien, plasmagestützten Strukturierung von Ultra-low-k Dielektrika für die Anwendung in einer 22 nm-Technologie und nachfolgender Technologien.
Das zweite Projekt beinhaltet die Verbesserung der Mikroprozessoreigenschaften mittels Einsatz von Kohlenstoff (Carbon Assisted Transistors).

study for ferroelectrical storages. In collaboration with GLOBALFOUNDRIES, the scientists at Fraunhofer CNT work on the optimization of **ALD processes for the manufacturing of high-k stacks**. Another important part of the research activities is the **analysis of high-k/metal gate layer in SRAM via atom probe tomography**.

Further projects were ordered by GLOBALFOUNDRIES like the **development of a wiring technology for minimum structures** considering the increasing requirements in electrical reliability as well as a project which focuses on process demonstrations of thin titan nitride layers using an ASM A412 100 waferbatch process for replacement gate.

Two other ongoing projects were already started before 2010. Fraunhofer CNT acts as subcontractor in both projects, which are financed by the Sächsische Aufbaubank (SAB).
The first project concentrates on the damage-free, plasma-enhanced structuring of ultra-low-k dielectrica for the application in the 22 nm technology and future technologies.
The second one comprises the enhancement of microprocessor properties using carbon (Carbon Assisted Transistors).

INNOVATION THROUGH COOPERATION

FRAUNHOFER-GESELLSCHAFT

Forschen für die Praxis ist die zentrale Aufgabe der Fraunhofer-Gesellschaft. Die 1949 gegründete Forschungsorganisation betreibt anwendungsorientierte Forschung zum Nutzen der Wirtschaft und zum Vorteil der Gesellschaft. Vertragspartner und Auftraggeber sind Industrie- und Dienstleistungsunternehmen sowie die öffentliche Hand.

Die Fraunhofer-Gesellschaft betreibt in Deutschland derzeit mehr als 80 Forschungseinrichtungen, davon 60 Institute. Mehr als 17.000 Mitarbeiterinnen und Mitarbeiter, überwiegend mit natur- oder ingenieurwissenschaftlicher Ausbildung, bearbeiten das jährliche Forschungsvolumen von 1,7 Mrd Euro. Davon fallen 1,4 Mrd Euro auf den Leistungsbereich Vertragsforschung. Zwei Drittel dieses Leistungsbereichs erwirtschaftet die Fraunhofer-Gesellschaft mit Aufträgen aus der Industrie und mit öffentlich finanzierten Forschungsprojekten. Nur ein Drittel wird von Bund und Ländern als Grundfinanzierung beigesteuert, damit die Institute Problemlösungen erarbeiten können, die erst in fünf oder zehn Jahren für Wirtschaft und Gesellschaft aktuell werden.

FRAUNHOFER VERBUND MIKROELEKTRONIK

Der Fraunhofer-Verbund Mikroelektronik (VµE) koordiniert die Aktivitäten der auf den Gebieten Mikroelektronik und Mikrointegration tätigen Fraunhofer-Institute.

Die Technologiekompetenz des Verbunds reicht von der klassischen CMOS-Technologie bis zum Einsatz innovativer Nanotechniken. Sie schließt neben Silizium auch Verbindungshalbleiter und neue Materialien ein. Die Kompetenz in der Entwicklung von CMOS- und anderen Bauelementetechnologien für die Mikroelektronik stellt die Basis sowohl für technologische Dienstleistungen als auch für anwendungsbezogene Komponentenentwicklung dar. Das Fraunhofer CNT ist Ansprechpartner für die Bereiche „More Moore“ und „Beyond CMOS“ im Geschäftsfeld Technologie.

FRAUNHOFER-GESELLSCHAFT

Research for practice is the main issue of all activities pursued by the Fraunhofer-Gesellschaft. The research organization, which was founded in 1949, undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration.

At present, the Fraunhofer-Gesellschaft maintains more than 80 research units in Germany, including 60 Fraunhofer institutes. The majority of the more than 17.000 employees are qualified scientists and engineers who work with an annual research budget of 1.7 billion euro. More than 1.4 billion euro of this amount are generated through contract research. Two thirds of the Fraunhofer-Gesellschaft's contract research revenues derive from contracts with industrial partners and from publicly financed research projects. Only one third is contributed by the German federal and Länder governments in the form of base funding which enables the institutes to work ahead on solutions to problems that will become relevant to industry and society in five or ten years.

FRAUNHOFER GROUP MICROELECTRONICS

The Fraunhofer Group for Microelectronics (VµE) coordinates the activities of Fraunhofer institutes working in the fields of microelectronics and microintegration.

The group's expertise ranges from classic CMOS technology to the use of innovative nanotechnologies. Apart from silicon, this also includes compound semiconductors and new materials. Expertise in developing CMOS and other device technologies for microelectronics forms the basis for both, technological services and application-specific component development. Fraunhofer CNT is the contact for the business area Technology which consists of two divisions: „More Moore“ and „Beyond CMOS“.

FRAUNHOFER IN DRESDEN: GEBALLTE FORSCHUNG

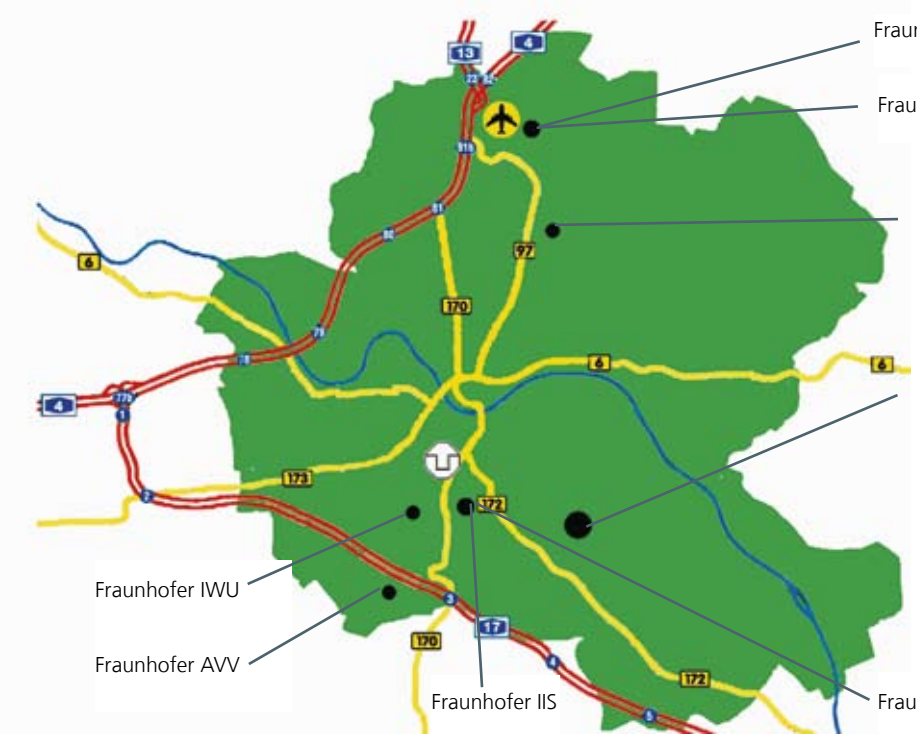
Die Fraunhofer-Gesellschaft ist mit sechs Instituten und sechs weiteren Einrichtungen in Dresden vertreten. Die zwölf Fraunhofer-Einrichtungen beschäftigen zusammen mehr als 1.100 Mitarbeiter bei einem jährlichen Umsatz von über 100 Mio Euro. Für die nächsten Jahre wird ein weiteres Wachstum prognostiziert.

Neben der außerordentlich hohen Dichte an Forschungseinrichtungen zeichnet sich der Standort Dresden durch eine enge Verflechtung von Industrie und Forschung aus. Die daraus entstehenden Spitzenleistungen und innovativen Entwicklungen setzen weltweite Impulse.

FRAUNHOFER IN DRESDEN: CLUSTERED RESEARCH

The Fraunhofer-Gesellschaft is represented in Dresden by six institutes and six other facilities. More than 1.100 employees work for the twelve Fraunhofer facilities. The annual turnover amounts to more than 100 million euro and further growth is expected within the next years.

In addition to the extraordinarily high density of research facilities, the region is characterized by the close connection between research and industry, resulting in the creation of leading-edge services and innovative developments which have a global impact.



INNOVATION THROUGH COOPERATION

CLUSTER NANOANALYTIK

Seit Oktober 2009 ist das Fraunhofer CNT Mitglied im Dresdner Fraunhofer-Cluster Nanoanalytik. Zehn Fraunhofer-Institute und drei Fakultäten der Technischen Universität Dresden sowie das Helmholtz-Zentrum Berlin bündeln ihre Kompetenzen und decken das gesamte Themenspektrum der Nanoanalytik ab. Die Institute sind flexibel vernetzt und werden auch sehr umfassenden Anforderungen im Bereich Analytik gerecht.

ALD LAB DRESDEN

Im Oktober 2010 wurde das ALD Lab Dresden gegründet. Mit dem Lab werden Kompetenzen auf dem Gebiet der ALD (Atomlagenabscheidung) am Standort Dresden, dem Institut für Halbleiter- und Mikrosystemtechnik (IHM) der Technischen Universität Dresden (Prof. Johann Bartha) und der ALD-Gruppe des Fraunhofer CNT (Dr. Jonas Sundqvist) zusammengeführt. Gemeinsam entwickeln die Partner neue ALD-Precursoren und –Prozesse für die Halbleiter- und Photovoltaik-Industrie.

E-BEAM-INITIATIVE

Seit April 2010 ist das Fraunhofer CNT offizielles Mitglied der E-Beam-Initiative.
Die Initiative bietet ein Forum für bildungs- und verkaufsfördernde Aktivitäten, unter dem Gesichtspunkt eines neuen „design-to-manufacturing"-Ansatzes, bekannt als „design for e-beam" (DFEB). DFEB reduziert Maskenkosten für Halbleiterbauelemente, in Verbindung mit Design, Design-Software, Herstellung, Herstellungsmaterialien und Hersteller-Software-Expertise.

CLUSTER NANOANALYTIK

Since October 2009, Fraunhofer CNT has been a member of the Fraunhofer-Cluster Nanoanalytics in Dresden. Ten Fraunhofer institutes, three faculties of the Dresden University of Technology as well as the Helmholtz-Zentrum Berlin consolidate their competences and thus cover the entire field of nanoanalytics. The institutes are flexibly linked and can meet comprehensive analytics requirements.

ALD LAB DRESDEN

The ALD Lab Dresden was founded in October 2010. It is a joint venture of the Institut für Halbleiter- und Mikrosystemtechnik (IHM) of the Dresden University of Technology (Prof. Johann Bartha) and the ALD group of Fraunhofer CNT (Dr. Jonas Sundqvist) which combines their competences in the field of ALD (atomic layer deposition). The workscope is to develop new ALD precursors and processes for the semiconductor and photovoltaic industry.

E-BEAM INITIATIVE

Since April 2010, Fraunhofer CNT is an official member of the e-beam initiative.
The initiative provides a forum for educational and promotional activities considering a new "design-to-manufacturing" approach known as "design for e-beam" (DFEB). DFEB reduces mask costs for semiconductor components linked to designs, design software, manufacturing, manufacturing materials and manufacturer's software expertise.

COMPETENCE AREAS AND RESEARCH RESULTS

Microelectronics is the basic technology for a lot of technical applications. The progress in the automobile and the computer industry can be owned by this technology. Microelectronic systems have to become smaller and smaller and more energy efficient. They also have to provide much more power and combine more and more new features. The key activities of Fraunhofer CNT focus on the development of innovative processes for high-performance transistors as well as the development of nanoelectronic integrated circuits to fulfill the tasks mentioned above. Fraunhofer CNT divides its groups into five areas of competences.

Analytics

Functional Electronic Materials - Front End of Line

Functional Electronic Materials - Back End of Line

Patterning

Devices & Integration

ANALYTICS

COMPETENCES

The competence area Analytics concentrates on the characterization of materials needed for the fabrication of modern semiconductor chips. It focuses on topics such as the distribution and activity of dopants, properties of surfaces and interfaces, crystallization and phase formation, lateral resolved stress measurements and quantification of impurities. In order to meet the challenges of ongoing miniaturization, we engage in the improvement of existing methods and also in the application of new methods, e. g. atom probe tomography.

TRENDS

In 2011, we plan to extend our activities in the field of atom probe tomography together with our partners Helmholtz-Zentrum Dresden-Rossendorf and Leibniz-Institut für Festkörper- und Werkstoffforschung Dresden. Fraunhofer CNT will offer preferred tool access to its partners under the intended platform of Advanced Atom Probe Laboratory Dresden and henceforth, Fraunhofer CNT will extend the usage of the atom probe tomography for material analysis outside the field of the semiconductor industry. Additionally, the atom probe tomography will be used in the publicly funded projects CoolAnalytics and HEIKO. In the frame of CoolAnalytics we shall characterize SONOS based NVM devices together with our partner X-FAB, while in HEIKO we will continue to study high-k/metal gate stacks with our partner GLOBALFOUNDRIES.

Group Manager Analytics: Dr. Lutz Wilde

Fraunhofer CNT
Competence Area Analytics

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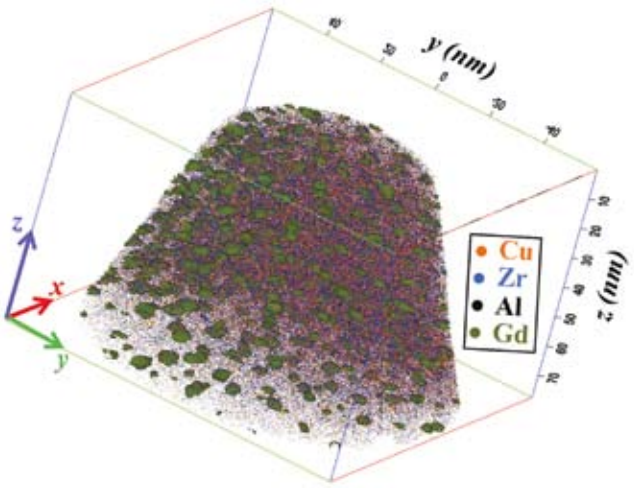
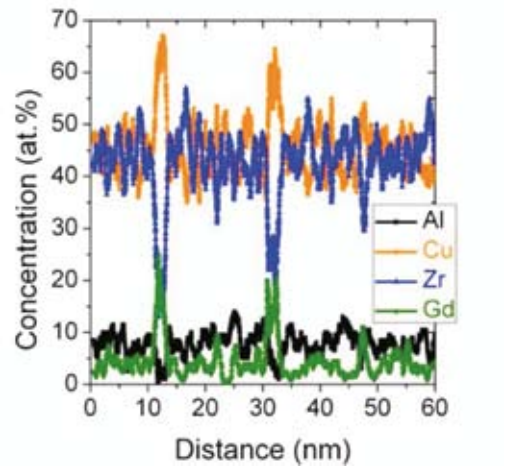
ATOM PROBE TOMOGRAPHY (APT) - PHASE SEPARATION IN $CU_{46}ZR_{47-X}AL_7GD_X$ METALLIC GLASSES

Cu-based bulk metallic glasses (BMG) have been shown to be excellent candidates for structural applications due to their high strength, high glass-forming ability (GFA), high thermal stability and inexpensiveness. Recently, it was detected that the addition of gadolinium dramatically increased the GFA of Cu-based alloys, and BMGs with a rod diameter of 10 mm could be obtained for $Cu_{46}Zr_{45}Al_7Gd_2$. Additions of Gd, however, provoke phase separation for rapidly quenched glassy $Cu_{46}Zr_{47-x}Al_7Gd_x$ alloys. The SAXS data shows the presence of compositional fluctuations with a dominant correlation length which is typical of early stages of spinodal decomposition (not shown here). The occurrence of phase separation in the $Cu_{46}Zr_{42}Al_7Gd_5$ metallic glass was confirmed by the APT investigations. Figure 1 shows the spatial distribution of the constituent elements for the as-cast state and iso-concentration surfaces for 10 at% Gd are drawn to elaborate the interface regions of the Gd-enriched clusters. The counted numbers of atoms by the APT data give the chemical composition $Cu_{46.1}Zr_{41.6}Al_{7.5}Gd_{4.8}$, which is in a good agreement with the nominal value. The 3D-APT micrograph clearly shows a heterogeneous structure with Gd-enriched clusters distributed throughout the analyzed volume having diameter in a range from 2 - 5 nm. The concentration profile from a cylinder of 3 nm in diameter through the volume is given in figure 2. The Gd-enriched clusters contain a relatively higher amount of Cu, however, are depleted in Zr and Al. The chemical composition of clusters with the highest Gd-content is about $Cu_{65}Zr_{15}Gd_{20}$.

(This work was performed in collaboration with Dr. Norbert Mattern from IFW Dresden, Institute for Complex Materials, Helmholtzstr. 20, 01069 Dresden, Germany.)



1 *Spatial distribution of the constituent elements of as-quenched glassy $Cu_{46}Zr_{42}Al_7Gd_5$ as analyzed by atom probe tomography. Iso-concentration surface 10 at% Gd is drawn in green to elaborate the Gd-enriched clusters for clarity, not 100 % of the atoms Cu [orange], Zr [blue] , Al [black] are shown).*

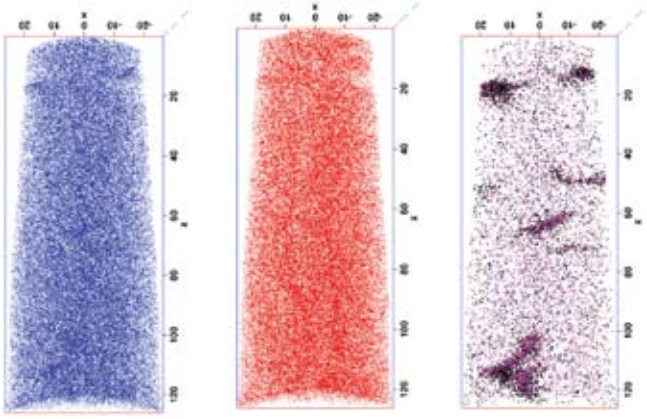


2 *Compositional depth profile of glassy $Cu_{46}Zr_{42}Al_7Gd_5$ from a selected cylinder of 3 nm diameter.*

ANALYTICS

OXIDE DISPERSION STRENGTHENED (ODS) HIGH-CR STEELS

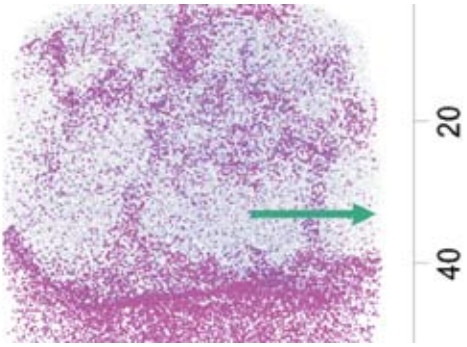
Oxide dispersion strengthened (ODS) steels are expected to increase the operation temperature of fusion reactor components. A model ODS-Fe-9%Cr alloy has been investigated using APT. It was produced by means of high-energy milling of elemental powders of Fe and Cr and commercial yttria powders. Compaction was based on spark plasma sintering. The finely dispersed oxides having dimensions in the nano-meter scale are known to improve the mechanical properties of ODS steels at high temperatures. APT measurements show yttrium oxide distributed in the FeCr matrix as shown in figure 1.
(These are initial results of a continued collaboration with Dr. Frank Bergner, Helmholtz-Zentrum Dresden-Rossendorf.)



1 *Atom maps of Cr (Blue), Fe (red), Y (pink) and oxide (black) showing distribution of yttrium oxide.*

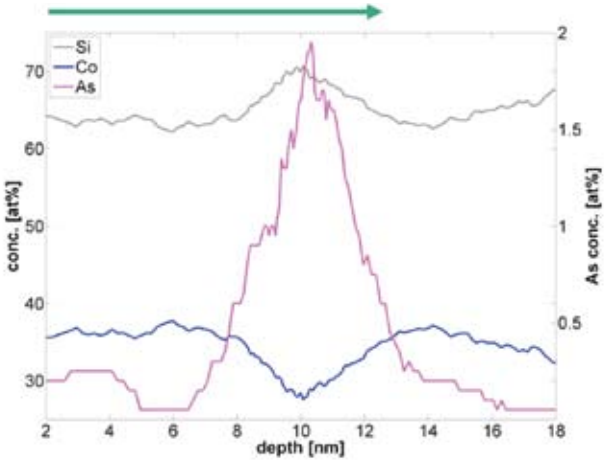
GRAIN BOUNDARY SEGREGATION OF ARSENIC IN $CoSi_2$/Si LAYER STACKS INVESTIGATED BY ATOM PROBE TOMOGRAPHY

Metal-semiconductor contacts in microtechnology are based on silicides, for example $CoSi_2$. One important step during fabrication is a clean Si surface prior to metal deposition as Co cannot even reduce a very thin layer of native oxide. An in-situ sputter etch is usually conducted to ensure a clean Si surface. Samples of $CoSi_2$ on arsenic doped (100)-wafer have been analyzed by atom probe tomography (APT) to study the influence of the cleaning process on the $CoSi_2$/Si interface.
Figure 1 shows an APT-reconstruction visualizing Arsenic as pink dots redistributed from the substrate into the Co silicide (Co blue dots, Si grey dots).
This sample depicts segregation of As to grain boundaries in the silicide. The rough interface $CoSi_2$/Si from the sputter etch probably enables the As diffusion via grain boundaries.



1 *A 3-dimensional APT reconstruction of a $CoSi_2$/Si layer stack showing grain boundary segregation of As.*

A small cylindrical volume placed across one of these grain boundaries enables the calculation of a concentration profile in this region (see arrow in figure 1). Figure 2 presents the resulting concentration profile. The As concentration at the grain boundary rises up to about 2 at% compared to nearly 0 at% inside silicide grains. The grain boundary itself exhibits a variation in Co and Si concentration as well. Arsenic atoms possibly occupy the Co lattice sites at the grain boundary during diffusion from the rough interface.



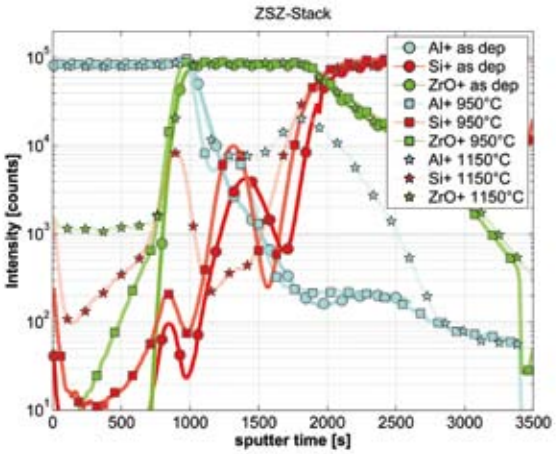
2 *Concentration profile of a grain boundary in $CoSi_2$, position indicated by an arrow in figure 1.*

SECONDARY ION MASS SPECTROMETRY

Time of Flight Secondary Ion Mass Spectrometry (ToF-SIMS) was used to characterize material stacks for the Gigascale Oriented Solid State flAsh Memory for EuRope (Gossamer, Grant agreement number: 214431) project. In this project, new material stacks for optimized overall memory cell performance parameters such as large program/erase window at lower program/erase voltages, fast program/erase operations, and reduced retention loss are developed from the TANOS approach. ZrO_2, ZrO_2/SiO_2 and ZrO_2/Al_2O_3 nanolaminates as charge trapping layer replace the commonly used Si_3N_4. These stacks reveal excellent program and erase performance, but a high retention loss emerging from intrinsic material properties was observed for all alternative stacks.

The physical properties of the planar material stack were investigated for intermixing or segregation effects after critical process conditions such as the Al_2O_3 post deposition annealing (PDA) at different temperatures via ToF-SIMS. All layers were analyzed from top (12 nm Al_2O_3) to bottom (Si-bulk).

The main effect which influences the electrical performance and especially the retention behavior is the diffusion of Zr and Si into the Al_2O_3 block oxide. The Si diffusion into the Al_2O_3 layer starts already at deposition conditions (275 °C). The Al_2O_3 layer has changed in its chemical and physical state after PDA at 950 °C and in particular at 1100 °C. This effect is responsible for the high retention loss. Hence, a stable Al_2O_3/ZrO_2 interface and adjusted PDA conditions are necessary to reduce diffusion effects.



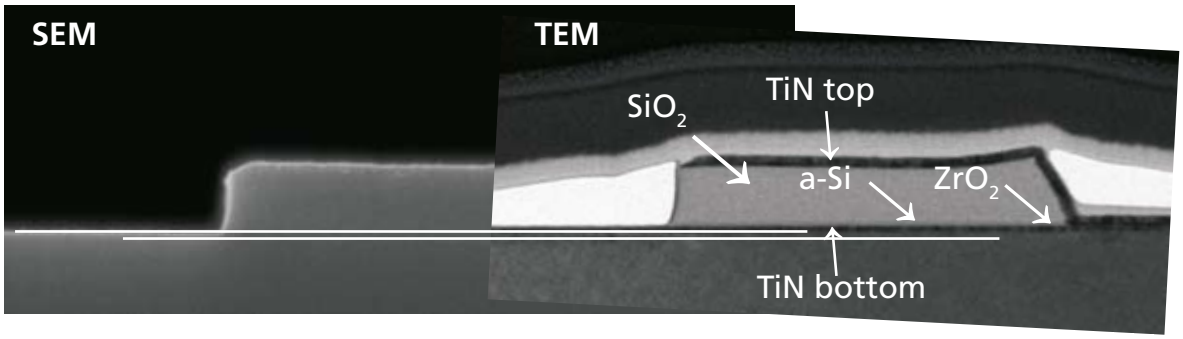
1 *ZSZ-stack analyzed with 500eV O_2+ sputter gun and 25kV Bi_3+ analysis gun. Strong diffusion of Zr and Si into the top Al_2O_3 is visible, increasing with temperature. The Zr is distributed uniformly within the Al_2O_3 while the silicon accumulates at its interface. Aluminum diffuses at high temperatures through the full ZSZ-stack to the bulk.*

ANALYTICS

ELECTRON MICROSCOPY

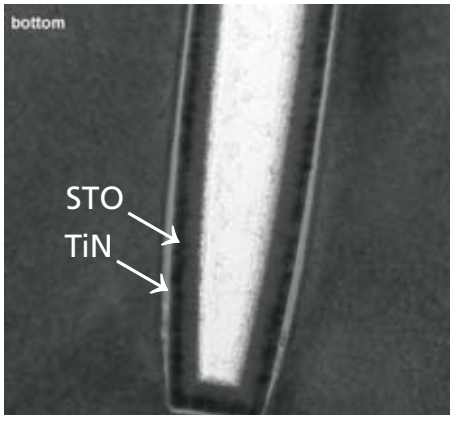
Electron microscopy (SEM and TEM) has been used to support the publicly funded project BRIDGE to study the material deposition and structuring processes for the formation of 2D & 3D MIM and 2D MIS structures. One example, as shown in figure 1, is the analysis of a 2D MIM structure. For electrical characterization purposes, the top electrode is contacted at a contact pad where the bottom electrode is separated from the high-k layer by a thin a-Si etch stop layer and a thicker SOG-SiO_2 layer.

These contacts are structured by a sequence of dry and wet etch processes, followed by subsequent ZrO_2 and TiN top electrode deposition. One question to be answered by electron microscopy was, if the etch processes caused a damage to the bottom electrode. As shown in figure 1 (left part), the topographical contrast of the SE detector of the SEM is not sufficient to give the correct answer. Therefore, a TEM investigation has been carried out (right part of figure 1). The TEM image clearly shows that the TiN bottom electrode remained undamaged after the etching processes.

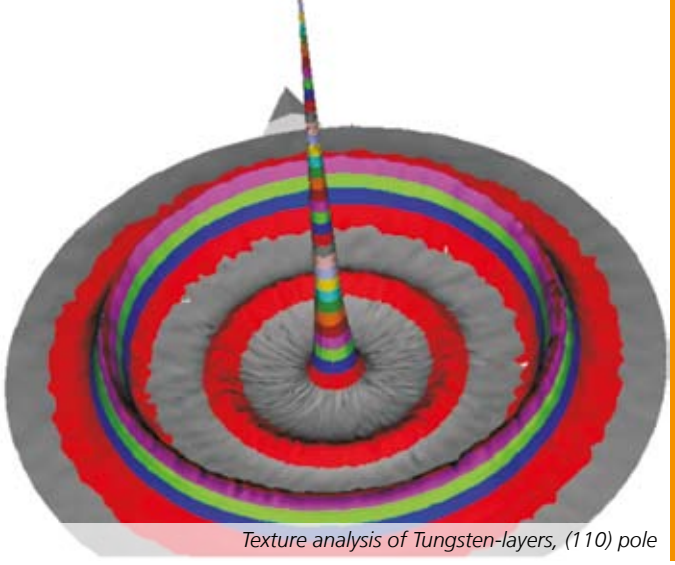


1 *Comparison of SEM and TEM image of 2D MIM structure; evaluation of etch processes.*

In the course of the BRIDGE project, the deposition of novel high-k dielectrics such as $SrTiO_3$ (STO) within trenches of a high aspect ratio of ~ 100 was studied.
In figure 2, the conformal deposition of a 12 nm STO film onto a 10 nm thin TiN electrode at the bottom of the trench is shown. By means of EDX, it was realized that the Ti:Sr ratio increases considerably with depth. There are several possible reasons for this which are mostly related to the Sr-containing precursor (lower sticking coefficient, thermal instability).



2 *TEM image of a deep trench filled with TiN bottom electrode and STO high-k layer.*



Texture analysis of Tungsten-layers, (110) pole

X-RAY DIFFRACTION & X-RAY REFLECTIVITY

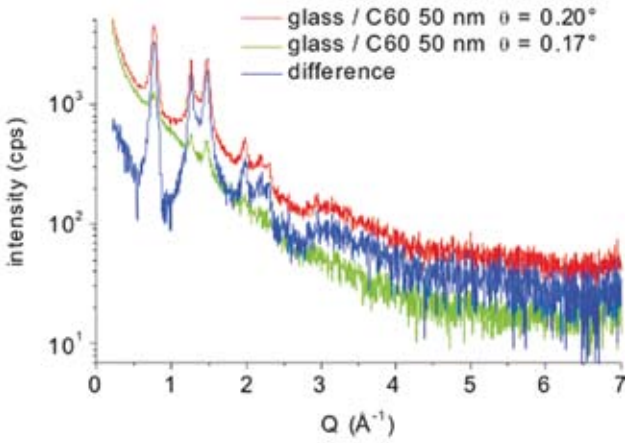
In 2010, the cooperation with external partners within the field of X-ray diffraction and X-ray reflectivity was successfully established. Together with Chris Elschner from TU Dresden, Institute of Applied Photophysics, 50 – 250 nm thin films of the Buckminster Fullerene C_{60} on glass substrate have been studied by means of grazing incidence X-ray diffraction. This material may be used as acceptor material in organic solar cells.

For the characterization of the short range order within the C_{60} films, the pair distribution function (PDF) was determined which describes the probability G(r) that two atoms have the distance of r to each other. In order to determine the PDF of this material, all scattering contributions from the substrate and from scattering in air need to be eliminated.

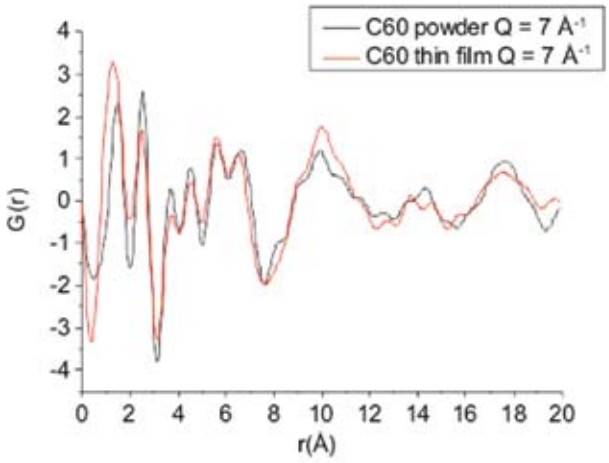
Therefore, two measurements per sample were taken, the first at the critical angle for total external X-ray reflection, where the penetration depth is below the layer thickness. A second measurement below the critical angle, resulting in an evanescent wave only, was taken to allow a background correction (see figure 1).

After applying further corrections, the reduced structure factor and subsequently the PDF were calculated according to the formula developed by Zernicke et al. [1]. The results were in excellent agreement with results obtained from C_{60} powder (see figure 2).

[1] Zernicke, F. & Prins, J. A., Z Phys. 41 (1927) 184.



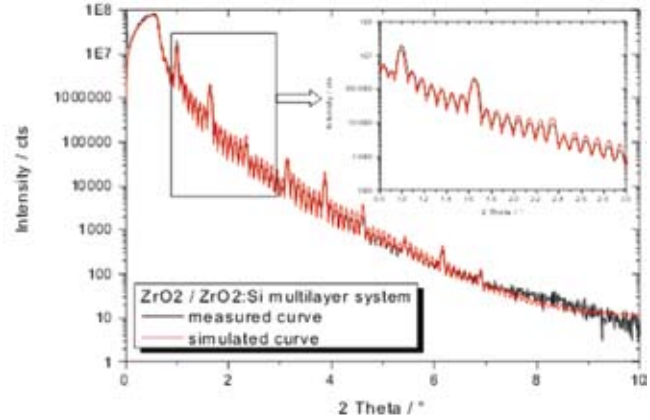
1 *Diffraction pattern of C_{60} thin films on glass substrate measure at & below critical angle (already converted to reciprocal space).*



2 *Comparison of the PDF of C_{60} powder (black line) and C_{60} thin film (red line); the whole diffraction pattern till Q = 7 Å-1 was used. The comparatively sharp peaks below 8 Å in the PDF correspond to intra-molecular distances (diameter of the C_{60} molecule is about 7.1 Å) whereas the broader peaks at higher distances correspond to inter-molecular distances. The broadness of these peaks can be explained by a rotational disorder of the C_{60} molecules.*

ANALYTICS

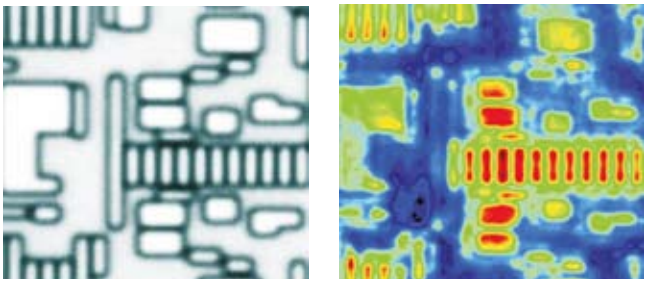
In cooperation with Frank Benner from namlab, X-ray reflectivity measurements have been carried out to determine the thickness, density and roughness of the individual layers within a n×(ZrO_2/Si:ZrO_2) multilayer stack which may be used as conversion layers to increase the efficiency solar cells. The films have been deposited by means of co-sputtering (PVD) with Ar onto ZrO_2 and Si target, respectively, at 100 °C substrate temperature. It is supposed that nanoscaled Si clusters are formed within the Si:ZrO_2 layers. From the analysis of the reflectivity curves, it can be concluded that the incorporation of Si into the ZrO_2 leads to a decrease the density by ~10 %. The roughness of both types of layers was less than 0.5 nm.



3 *Reflectivity curve (black line) and best fit (red line) of an as deposited 7×(ZrO_2/Si:ZrO_2) multilayer stack on Si substrate with a total thickness of ~ 85 nm. The thickness of the Si: ZrO_2 layers is ~ 8.1 nm, the ZrO_2 layers are around 3.5 nm thick.*

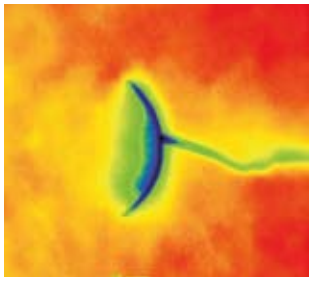
RAMAN SPECTROSCOPY

Optical measurements provide a comprehensive, fast and non destructive characterization of devices and structures for the microelectronic, semiconductor or solar industry. By means of Raman spectroscopy, it is possible to analyze vibrations in crystalline solids regarding their frequency, intensity and distribution. Hence, a number of properties like stress, orientation, composition, film thickness, crystal structure and temperature can be measured on different materials. Stress plays a crucial role in any application involving semiconductor materials. A STI (shallow trench isolation) structure of a modern DRAM device was analyzed regarding its stress state induced by the patterning of the silicon substrate and the filling with silicon oxide. A laser beam is focused onto the sample and the sample is scanned in x and y. The LO (longitudinal optical) phonon mode of silicon is detected by the spectrometer and analyzed regarding intensity and frequency. Changes in the frequency can be correlated to the stress state in the crystalline silicon with high spectral and spatial resolution. Thus, it is possible to get a point by point measure of the stress state in a real microelectronic structure (see figure 1).

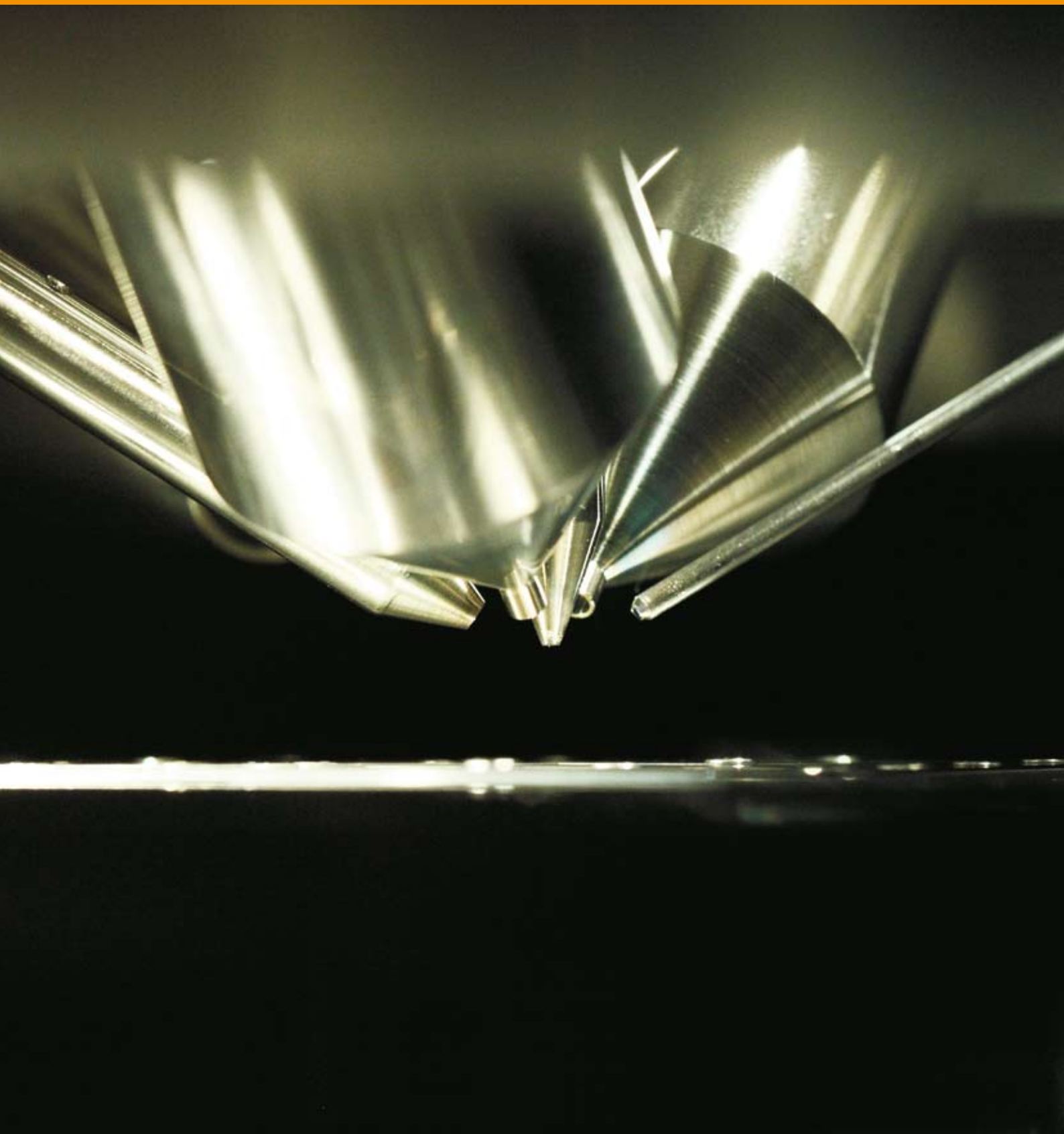


1 *Left: microscope map of STI-structure, Right: stress map obtained by Raman microscopy with high compressive stressed regions (red) and tensile stressed regions (dark blue).*

Other measurements were made on samples used in solar cell manufacturing. Here, high stress states can be visualized to find possible causes for defects like cracks or delamination (see figure 2).



2 *Stress map of silicon film used in thin film solar cells, showing high compressive material (red) and relaxation of stress by crack formation (blue/green).*



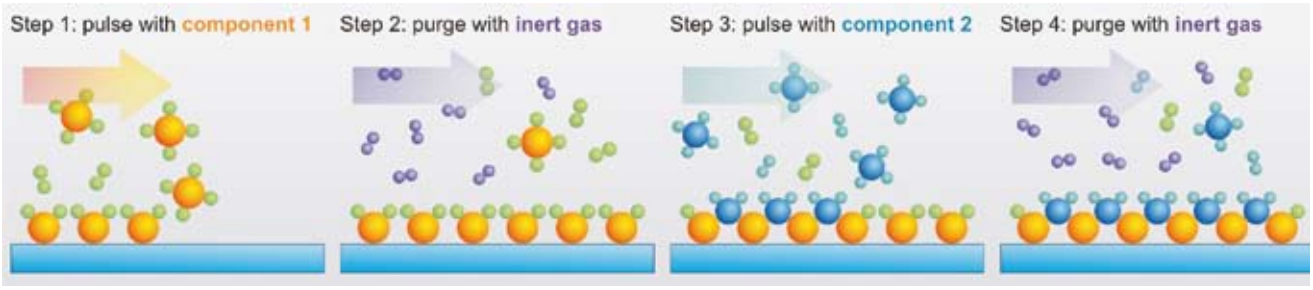
FUNCTIONAL ELECTRONIC MATERIALS - FRONT END OF LINE

COMPETENCES

Objective of this research area is the development of insulating, semi-insulating and conductive thin films. These materials are suitable for various applications in micro- and nanoelectronics.
One of the core competencies of the group is the Atomic Layer Deposition (ALD) of dielectric and conductive layers on 300 mm silicon wafers. The broad spectrum of ALD research activities covers different technical areas: ALD precursor testing, hardware and equipment evaluation as well as material and process development for high-volume manufacturing. Fraunhofer CNT works in close collaboration with industrial and academic partners. Hence, the Dresden ALD community established the „ALD Lab Dresden" as a common platform in fall 2010.

TRENDS

The major topic of our R&D activites is high-k dielectrics and metal gate materials for gate stacks in future generation field effect transistors (FET). In addition, we continue our activities in the evaluation of ferroelectric materials for FeFET memories.
In 2010, a low thermal budget process for selective epitaxial growth (SEG) of SiGe was successfully developed on a 300 mm large batch furnace. Beside the usage in microelectronics (channel material, source/drain stressor), the concept of batch epitaxy is of particular interest for low cost applications such as thin film photovoltaics.



1 *The ALD cycle of a metal oxide deposition is composed of the following steps: metal-containing precursor pulse (step 1), purge of non-reacted precursor and reaction products with inert gas (step 2), oxidant pulse e.g. ozone or water (step 3) and a second inert gas purge to remove reaction products (step 4). The sequence is repeated several times to achieve the desired film thickness.*

Group Manager Functional Electronic Materials - FEoL: Dr. Malte Czernohorsky

Competence Area
Functional Electronic Materials - Front End of Line

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„ALD LAB DRESDEN“ - RESEARCH COOPERATION ON ULTRA-THIN FILMS BY FRAUNHOFER CNT AND TU DRESDEN

ALD Lab Dresden

Fraunhofer CNT develops advanced process steps for manufacturing in nanoelectronic applications on 300 mm wafers. The Atomic Layer Deposition (ALD) is one of the key process technologies of the institute. In the ever growing market of thin film technology, ALD plays a unique role. The self-limited deposition of atomic layers enables conformal coating of arbitrary surfaces and allows exact thickness control on atomic level. ALD is the method of choice, especially when conventional deposition technologies (e. g. CVD, PVD) are at their limits in terms of step coverage and thickness uniformity.

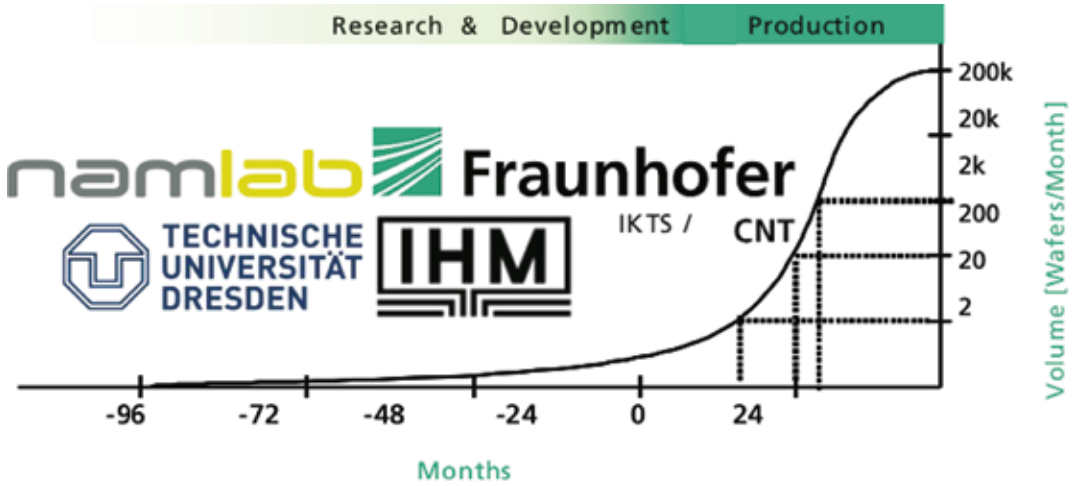
Industrial adoption of the ALD technology is already on its way for applications in nanoelectronic devices with aggressive architectures such as three-dimensional metal-insulator-metal capacitors (3D MIM Caps) for stand-alone and embedded DRAM as well as for leading edge CMOS high-k/metal gate transistor technology. Today, in leading edge commodity and high-end memory and logic products on 300 mm wafers at least one film is generated by ALD. This technology is currently driving the development forward for the next generation of technology nodes and has even contributed to accelerate Moore´s Law.

Apart from the application in nanoelectronics, ALD is a key enabling technology for the innovation in several technological fields of nanotechnologies but driven by the semiconductor industry. ALD has been able to gain a wider spectrum of applications, e. g. in the photovoltaic industry.

The concept of the ALD Lab Dresden is to join forces between two institutes with long term experience in ALD in Dresden: The Institute of Semiconductor and Microsystems Technology (IHM) at Dresden University of Technology (Prof. Johann Bartha) and the ALD group at Fraunhofer CNT (Dr. Jonas Sundqvist). Under the umbrella organization of "ALD Lab Dresden”, they seek to formalize the collaboration in the field of ALD which has already been existing for five years.

“Together we are developing new ALD precursors, processes and process technologies with focus on the semiconductor and photovoltaic industry” says Dr. Jonas Sundqvist, ALD expert at Fraunhofer CNT. “Using the advanced in-situ and clustered analytics at IHM, we can gain a deeper understanding of the ALD process. Such information is proven most beneficial when scaling up research results for production level ALD processing."

FUNCTIONAL ELECTRONIC MATERIALS - FRONT END OF LINE



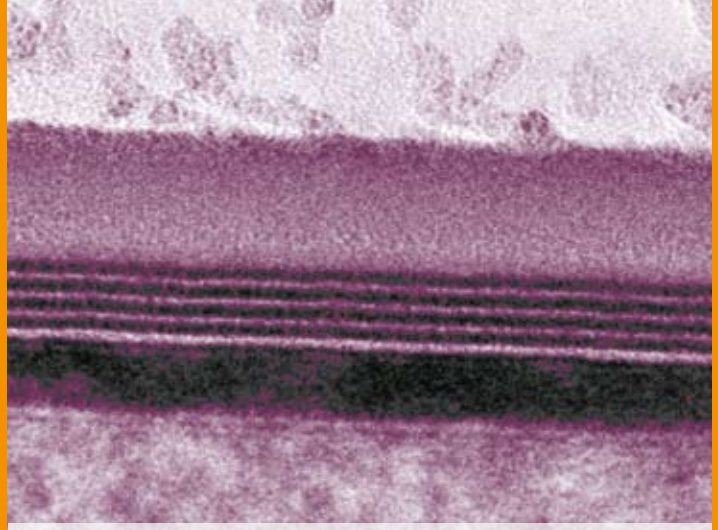
1 *Concept of the ALD Lab Dresden: Academic partners (TU Dresden IHM, namlab) focus on basic materials research. Fraunhofer (CNT, IKTS) transfer the research results into 300 mm manufacturing.*

"For the scale up task we will use both custom made equipment of common design available at both our labs, and state-of-the-art production proven ALD processing equipment, Pulsar 3000 and A412 Large Batch ALD from ASM that is available at Fraunhofer CNT." Working in close collaboration with chemical suppliers, e. g. Air Liquide, the ALD Lab Dresden will develop new precursors and processes for the industry. By using Fraunhofer CNT's production level fab infrastructure, the ALD Lab Dresden will be able to transfer research results most efficiently into a manufacturing environment by offering pre-qualified ALD process technology and precursors for regional and global industrial customers.

HIGH-K METAL GATE (HKMG) TRANSISTOR TECHNOLOGY

Today's high performance leading edge CMOS digital logic is fabricated in high-k metal gate (HKMG) technology using hafnium-based high-k materials for the gate insulator.
For decades, CMOS transistor gate stacks consisted of SiO_2 or later SiON dielectrics and poly-silicon gates. The scaling of geometrical device dimensions was the method of choice to push device performance from generation to generation. The dielectric thickness of the transistor eventually dropped below 2 nm. Thus high gate leakage currents dominate and the static power dissipation of the integrated circuit increased unacceptably. Dielectrics with higher dielectric constant (high-k) in combination with metal gates enable scaling below 1 nm equivalent oxide thickness (EOT) while maintaining low leakage currents.

The scientists of Fraunhofer CNT work in close cooperation with the long-term partner GLOBALFOUNDRIES on the optimization of ALD processes for the manufacturing of high-k stacks. Deposition process and material properties of the high-k dielectric and the underlying base oxide



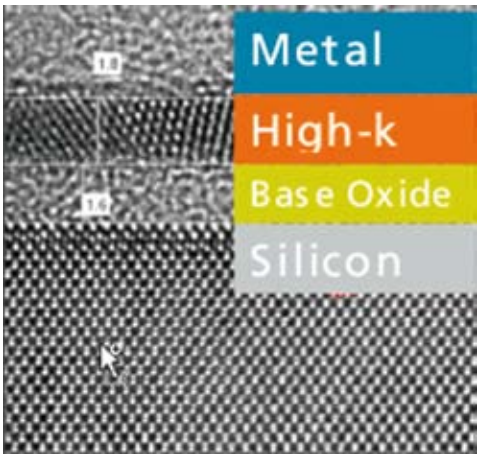
TEM image of a nanolaminate consisting of ZrO_2 and SiO_2

need to be improved to fulfill reliability requirements. In addition, new metal gate materials for the metallic gate electrode are evaluated to implement new integration schemes.

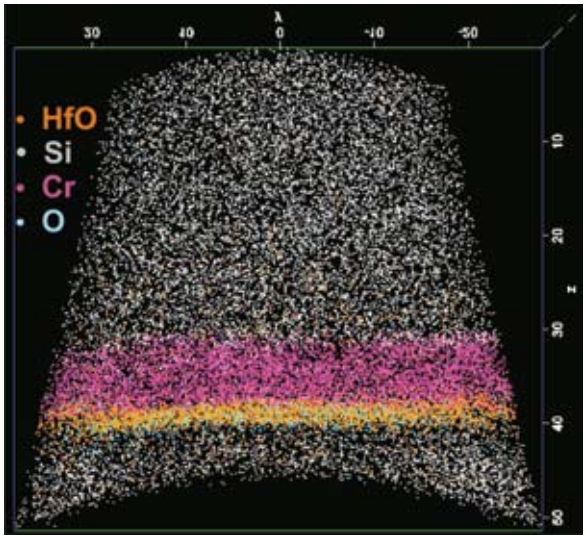
Fraunhofer CNT announced its participation in the new research project "HEIKO" which started in 2010. The project is funded by the Sächsische Aufbaubank (SAB) and the European Fund for Regional Development (EFRE) with an amount of 3.8 million Euro and deals with the development of future high-k gate dielectric transistors including a feasibility study for ferroelectric storage.

An important part of the research comprises the analysis of high-k/metal gate layers in SRAM via atom probe tomography. The atom probe tomography will be realized by an atom probe. This tool permits a 3-dimensional picture of a probe as well as its chemical analysis on atomic level. Atoms can be visualized on a 3-dimensional picture by marking them with color coding. Thus, the transitions of high-k and metal-gate layers can be shown clearly.

In the course of another sub-project and in cooperation with namlab, the specialists of Fraunhofer CNT investigate the usability of ferroelectric material in the gate layer stacks of a ferroelectric field effect transistor (Fe-FET). The manufacturing and the structuring of this coating system requires the optimization of the Atomic layer deposition (ALD) for ferroelectric material and metal electrode as well as the individual process development of an adequate dry etching procedure.
FeFET combines advantages of different memory concepts, the fast access of DRAM and longtime data storage of non-volatile memories.



1 *Cross section TEM image of a high-k/metal gate stack. The gate insulator consists of a base oxide and the actual high-k dielectric. Image source: GLOBALFOUNDRIES*

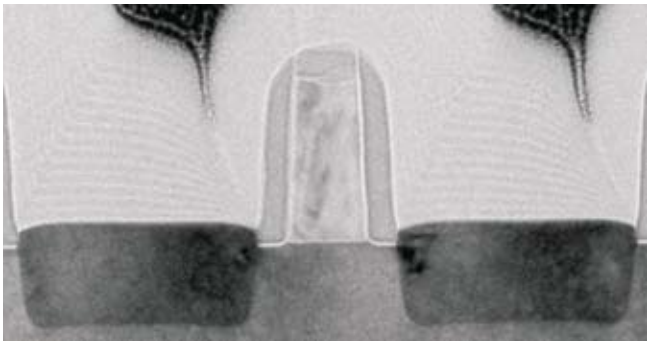


2 *3-dimensional atom map of a high-k layer. Cr and Si act as a protection layer during sample preparation. The depth profiles of three samples were measured in a similar way. Image source: GLOBALFOUNDRIES*

FUNCTIONAL ELECTRONIC MATERIALS - FRONT END OF LINE

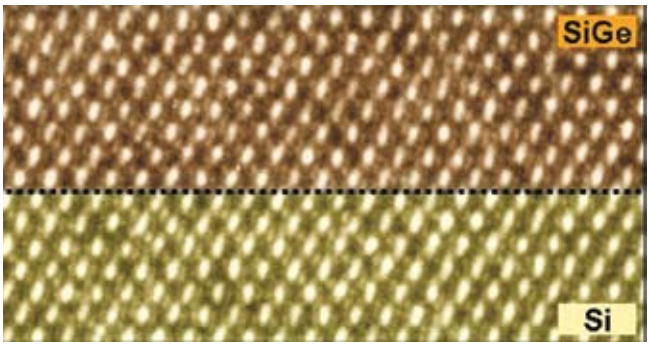
SiGe EPITAXY ON A 300 MM BATCH FURNACE

Epitaxy has become more and more important for state-of-the-art CMOS manufacturing technology and this trend is expected to continue in the foreseeable future. Strain engineering by Si/SiGe epitaxy is used for charge carrier mobility enhancement in high performance devices. Additionally, in-situ doped source and drain epitaxy enables the realization of very abrupt p/n-junctions. For 32 nm and 28 nm node high-k metal gate (HKMG) technologies, epitaxially-grown SiGe transistor channels are introduced to hit VTT targets for the pFET.



1 *TEM image of a p-channel MOSFET with embedded SiGe source and drain. The SiGe induce compressive strain in the transistor channel enhancing charge carrier mobility.*

Even though epitaxy is of large benefit for a variety of technologies, the usual high cost of ownership prevents a wide market penetration for several main stream technologies. By using vertical batch furnaces for epitaxy in 300 mm high volume manufacturing significant cost reduction is possible and thus will enable new applications such as silicon based photovoltaic power generation.
Fraunhofer CNT investigated the feasibility of epitaxial silicon and silicon germanium growth on a commercial large batch vertical furnace.



2 *High resolution TEM image of the interface between epitaxial silicon germanium layer on a silicon (100) substrate.*

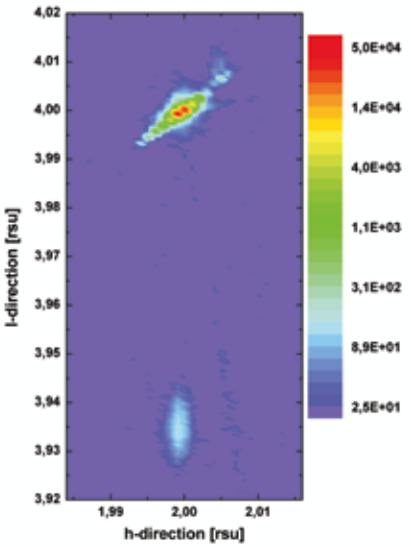
The gas supply of this furnace was modified to provide the necessary precursor chemistry for the growth of silicon and germanium. Additionally, the furnace hardware was modified to enable higher process temperatures. The temperature controller was trained to guarantee the necessary temperature stability during the wafer processing.

To enable epitaxial growth, it is absolutely necessary to completely remove the native oxide from the wafer surface. Before loading the wafer batch into the furnace, the native oxide is removed by wet cleaning with dHF.

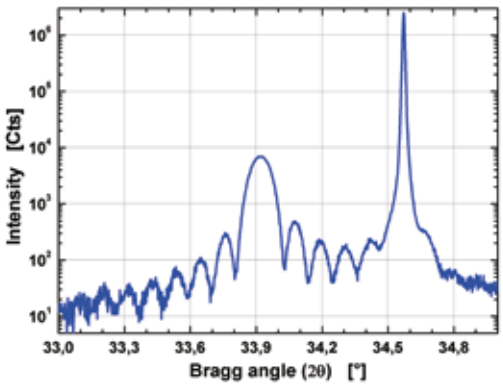
Additionally, an in-situ clean uses an hydrogen treatment before the epitaxy has been developed to remove the last traces of oxygen from the wafer surface. ToF-SIMS analysis verifies the efficient removal of oxygen at the interface between silicon substrate and epitaxially grown layer. Such an in-situ cleaning is necessary for the growth of high quality silicon or silicon germanium layers. AFM shows very smooth surfaces after growth (<0.2 nm RMS). HRXRD reveals sharp layer peaks and well defined thickness fringes indicating high crystal perfection. XRD and Raman spectroscopy indicate fully strained layer after growth.

The layer composition of the SiGe can be adjusted easily by altering the precursor mix. Germanium concentrations of the SiGe layers from 8 to 32 at% were demonstrated. With spectroscopic ellipsometry the uniformity was analyzed. Due to the wafer rotation, a rotational symmetry was found and the layer thickness and the germanium concentration increased from wafer center to wafer edge due to precursor depletion across the wafer.
On a 200 mm sibling of the 300 mm furnace, selective epitaxial growth was tested with dichlorosilane in hydrogen at 675 °C growth temperature in an earlier study. For this test, patterned wafers with an oxide hard mask were used. SEM imaging shows the selective growth on silicon only, while growth on the oxide is effectively suppressed. However, this was not yet tested on the 300 mm hardware.

This proves that epitaxy of silicon and silicon germanium on a vertical batch furnace is a feasible option for semiconductor high volume manufacturing and especially due to the significant cost of ownership reduction such a process can enable epitaxy also for cost sensitive markets.



3 *HRXRD reciprocal space map of a SiGe layer on Si substrate. The alignment in h-direction confirms that the epitaxial SiGe layer is fully strained.*



4 *HRXRD ω-2θ-scan of an epitaxial SiGe layer on Si substrate. The sharp peak and thickness fringes indicate high crystal quality.*

FUNCTIONAL ELECTRONIC MATERIALS - BACK END OF LINE

COMPETENCES

The group Back End of Line (BEoL) was established in May 2010 at Fraunhofer Center Nanoelectronic Technologies and is equipped to enable a full 300 mm copper metallization process. The process flow starts with an Applied Materials dry etch tool, followed by a Semitool single wafer cleaning tool, an Applied Materials CVD/PVD sputter tool, a Semitool single wafer plating tool, a Tokyo Electron anneal oven and ends with the Applied Materials chemical-mechanical polishing (CMP) tool. The ILD deposition and the lithography is carried out usually by our industry partner GLOBALFOUNDRIES as well as in house using our e-beam system.

The general topics range from testing of new chemicals for copper plating, post etch cleaning and CMP processes. Besides process development, we validate novel barrier materials like Ruthenium or Cobalt and investigate damage-free plasma processes for carbon containing ILD materials. To support our research, a broad range of analytical in-line and ex-situ tools are available like an atomic force microscope (AFM), an ellipsometer, a CD-SEM and more. In addition, unique analytical tools like an in-situ x-ray fluorescent spectrometer (XPS), an ellipsometric porosimeter (EP) or inline plasma analytics exist.

TRENDS

The metallization process experienced a lot of of changes during the last two decades. The main changes are the replacement of aluminum by copper and the change from silicon dioxide as the interlayer dielectric (ILD) to carbon containing porous ILDs. With decreasing pattern size, the change and adaption of existing processes to fulfill the technological requirements are the main topics.

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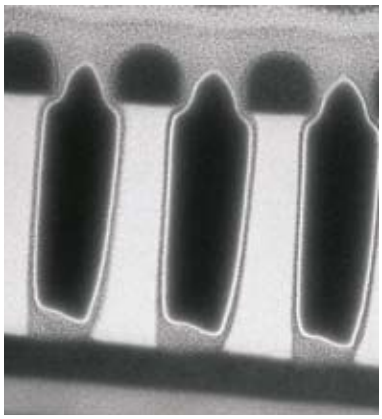
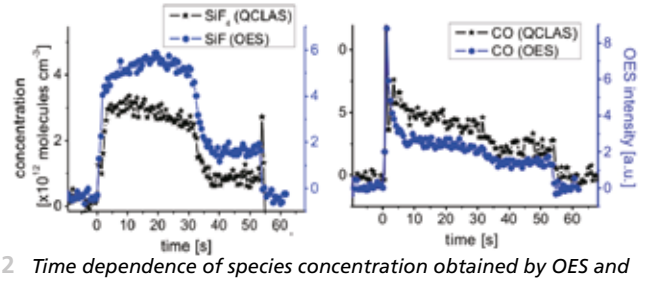
ADVANCED PLASMA ANALYTIC FOR ULTRA LOW-K (ULK) DIELECTRIC PATTERNING

To decrease the line-to-line capacitance in leading edge ultra large scale integrated circuit structures, low-k dielectrics as well as porous ultra low-k (ULK) materials are being introduced in the back end of line flow. It is crucial to gain further understanding in which way different plasma parameters, like source and bias power or gas mixtures and additives alter the trench profile and influence the degradation of the ULK dielectric. In-situ plasma diagnostic is an important tool to detect and to monitor process related dependencies and to correlate them with results of ex-situ analysis, like SEM.

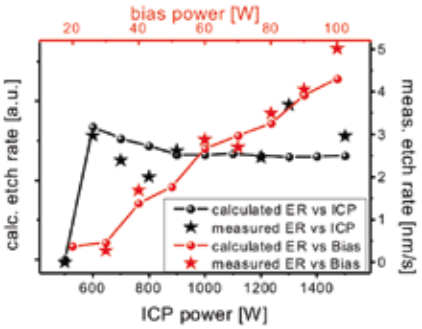


1 *EFTEM view of a 45 nm node ULK stack after trench lithography mask opened.*

In a study, which is part of a joint project with GLOBALFOUNDRIES, it was shown that optical emission spectroscopy (OES) can be used to predict certain trends in the etch profile variation during a typical fluorocarbon based etch process. A model was developed to estimate the trench profile after ULK etch by in-situ OES measurements. It is furthermore validated by consistent results from mass spectrometric measurements (QMS) and quantum cascade laser absorption spectroscopy measurements (QCLAS) (see figure 2). Most important, it could be verified by measuring the trench profiles with the help of SEM views (see figure 3).

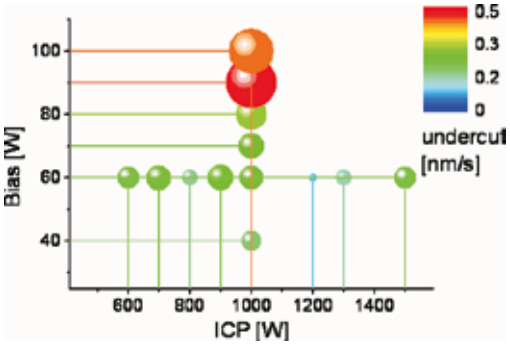


2 *Time dependence of species concentration obtained by OES and compared to absolute concentration measurements by QCLAS.*



3 *Etch rate dependence on ICP and bias power calculated with the help of in-situ OES and compared to actual trench depths measured by SEM. An excellent qualitative correlation is apparent.*

Sidewall damage in the ULK dielectric can be measured by different techniques such as electron energy loss spectroscopy (EELS) or energy-dispersive x-ray spectroscopy (EDX). These methods might not be sensitive enough for small damage regions, hence ULK sidewall damage was characterized by post HF-dip SEM measurements (see figure 4).



4 *Amount of trench sidewall damage in dependence of ICP and bias power. No clear dependence on ICP power is visible, while the damage clearly increases with increasing bias power.*

Inside view of the cleaning tool.

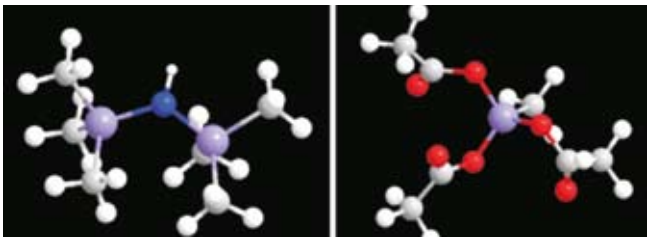
CLEANING

For cleaning of pattern structures a multi-chamber tool for 300 mm wafers is available. The tool includes the possibility of water-based (acid or base) and solvent based cleaning processes. Different chambers are available for this purpose, basic chambers like the capsule and special chambers like the backside clean, the spray or the ultrasonic chamber.

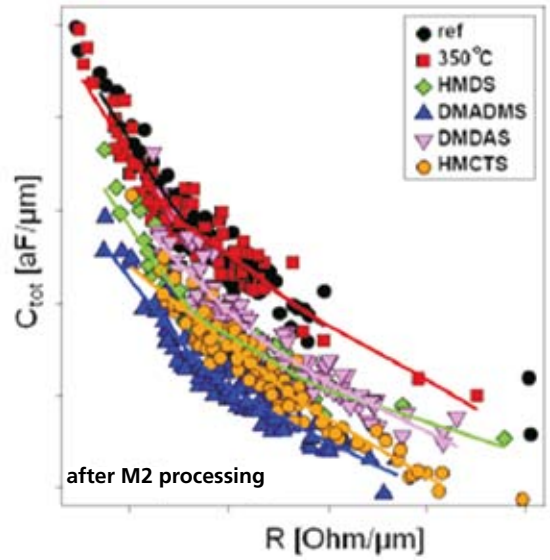
Beside standard cleaning processes, several studies with different chemical vendors like ATMI, Convidien, DuPont or Kanto for ILD in combination with additional requirements like compatibility with metal hard mask materials (Titanium nitride) or copper diffusion layers (cobalt-wolfram-phosphorus) have been done.

DIELECTRIC REPAIR

The damage of porous ultra low-k (ULK) dielectric is a big challenge. Since there has been no damage-free plasma processing possible, an alternative way was developed to restore the properties of the pristine ULK dielectric. The main problem of the plasma treatment is the formation of so-called silanol groups (Si-OH) on which water can be easily adsorbed. This causes an increasing k-value and degradation of the electrical properties of the ILD material. Therefore, a vapor-phase-based repair process was developed. Several silylation chemicals were tested as shown exemplarily in figure 1. Those chemicals contain reactive groups which take over the hydrogen atom of the silanol groups. In exchange, a non-polar metyhlsilyl group is bonded on the oxygen atom of the silanol group. This process was found to restore the k-value and reduce the leakage current and the amount of depleted carbon to a significant amount and it provides a surface free energy comparable to that of the pristine film. In pattern structures the resistance-capacitive (RC) behavior was improved by more than 10 % in comparison to the structures with no treatment as shown in figure 2. This improvement of the electrical behavior of the interlayer dielectric will result in an improved circuit switching, meaning a lower signal delay and a lower energy consumption of the final chip.



1 *Two sample chemicals for ULK repair.*

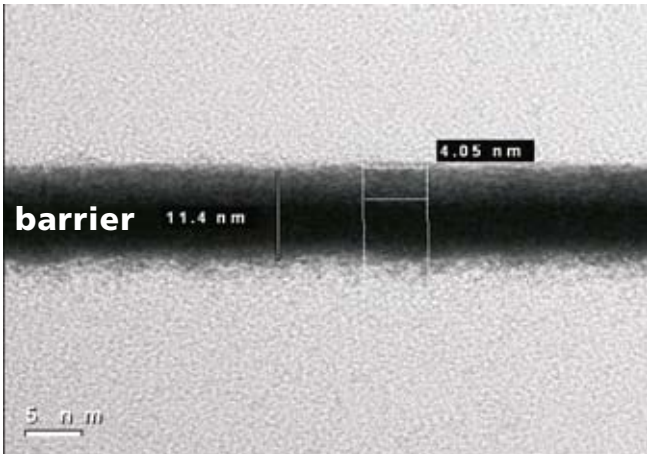


2 *RC behavior with and without repair step.*

FUNCTIONAL ELECTRONIC MATERIALS - BACK END OF LINE

BARRIER/SEED DEPOSITION

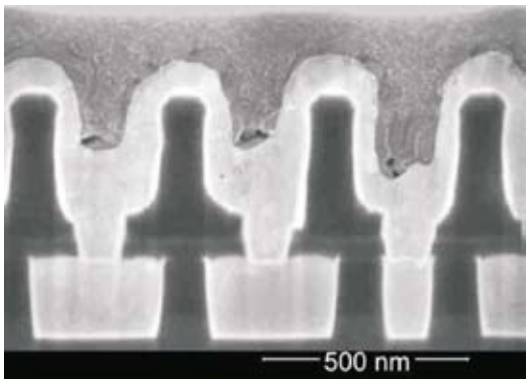
A critical parameter for the performance of the wiring within a microchip is the diffusion barrier. In conventional systems, first tantalum nitride and then tantalum is deposited by sputtering in a physical vapor deposition (PVD) chamber. Afterwards, the wafers will be transferred within the deposition cluster to a copper seed PVD chamber. The seed is essential for the following copper plating. With new barrier materials, like chemical vapor deposited (CVD) cobalt as a seed repair layer, it is possible to adopt the seed functionality. This is particularly important for very thin copper seed layer and can be realized at the new Cu Rf(x) chamber at Fraunhofer CNT. Also, a second barrier PVD chamber allows the testing of other promising material systems like Ta(N)Ru layers.



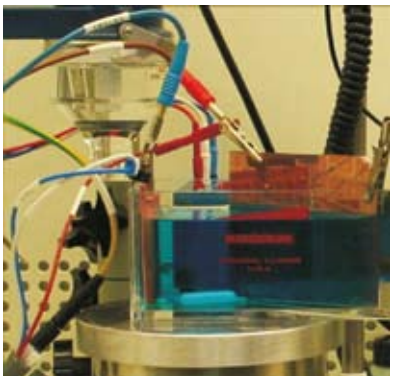
1 *CVD cobalt barrier on tantalum nitride layer.*

ELECTROCHEMICAL DEPOSITION

In the semiconductor industry copper is used as the favorite material for interconnects in microprocessors for more than a decade. Since the electrochemical filling of etched structures has been crucial for the integrity of the circuits, the investigation of the bath chemistry is a main topic at Fraunhofer CNT. By adding organic-based additives, the process can be controlled that the structures will be filled straight from bottom to top, the so called „super filling" behavior. Thus, it is possible to produce void free copper filled vias and lines. At Fraunhofer CNT, the filling process is improved by controlling the current regime and selecting the additive chemistry. Hence, it is possible to develop better models and optimize the processes.



2 *SEM image of partial filled structures.*



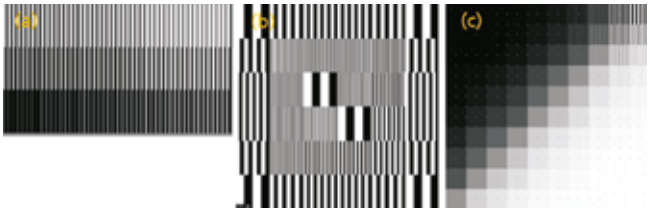
3 *Hull cell for coupon plating tests.*

FUNCTIONAL ELECTRONIC MATERIALS - BACK END OF LINE

CHEMICAL-MECHANICAL PLANARIZATION (CMP) – PROCESS AND SIMULATION

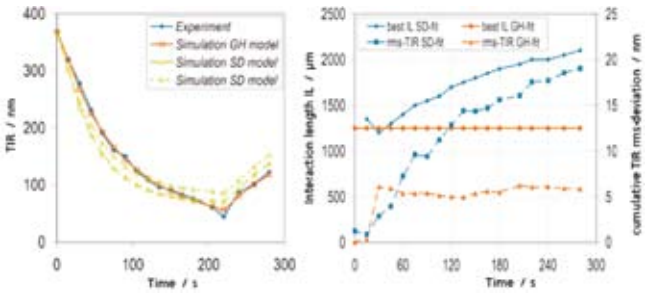
As the size of modern integrated circuits (IC's) continues to shrink, the planarity of structures after CMP becomes more and more crucial. A better understanding of the relevant mechanisms affecting planarization is needed in order to meet future process specifications. One of the problems that have attracted many research and modeling activities is the within-chip non-uniformity of polished oxide and nitride film stacks in IC fabrication which affects the functionality of the circuit. The non-uniformity arises from a pattern-dependence of the planarization. In order to predict this pattern-dependence to optimize the CMP process and if needed to modify the chip design, chip-scale CMP models are needed.

In several studies which where part of a joint project with GLOBALFOUNDRIES, TU Dresden and the Leibniz Institute of Polymer Research Dresden, the planarization behavior of patterned wafers was in the focus of research. Thereby, the influence of structural parameters and consumables on the topology evolution was systematically examined and modeled using specifically developed CMP test-wafers (figure 1) and analysis routines.



1 *Structures used for process characterization. (a) Density field 1 (14 x 8 mm), (b) pitch field (14 x 14 mm), (c) density field 2 (20 x 20 mm), white: up-regions, black: down-regions. The density fields contain 18 or respectively 100 macros (2 x 2 mm) with distinct pitch and nominal densities as defined in the sketch ranging from 0 % to 100 %. The pitch field contains 36 macros (2 x 2 mm) with approximately 50 % density and a variety of pitches.*

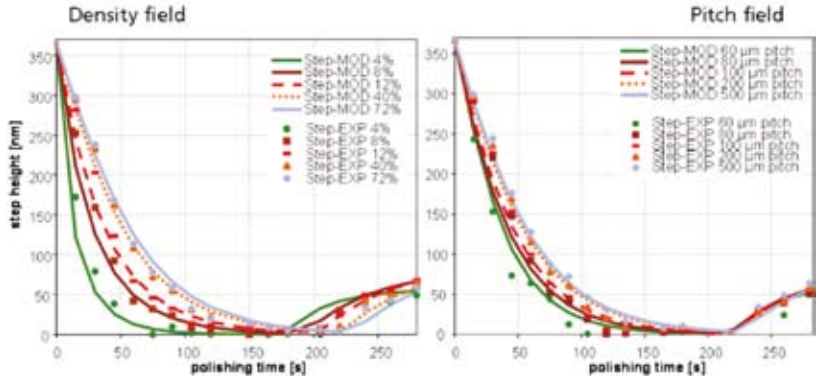
Several CMP models have been developed. One of them is the global heights (GH) model that incorporates the effects of pressure distribution between areas with different density on the chip due to height differences on large length scales, both, initially present or arising during the planarization process. It has been shown that the continuous reevaluation of the wafer-pad-contact force balance for the changing height values arising at every numerical time step in the calculation leads to a qualitative and quantitative improvement. This has been demonstrated especially for the fit of the global height differences on the chip (TIR) which is a central process metric in production (figure 2). Moreover, compared to conventional CMP models, the new global heights model allows an improved coupling to geometric models for the initial topography that describe effects of the deposition process.



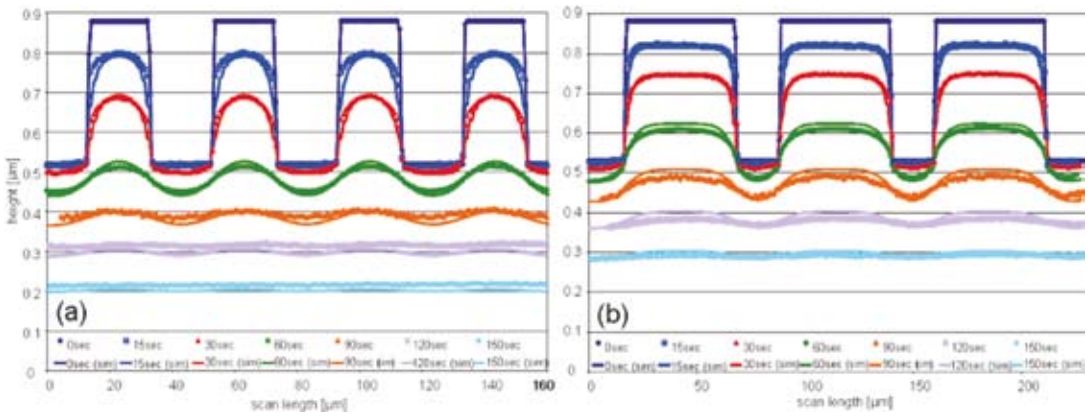
2 *(a) Comparison of experimentally measured TIR (symbols) to model predictions. (b) In contrast to conventional CMP models, the best fit of the GH model to the experimental data can be obtained by using a constant value for the interaction length (IL) between wafer features.*

In spite of the large focus on pattern density, a significant variation with pitch has also been observed in oxide CMP which turns out to be closely related to the characteristic roughness of the polishing pad produced during conditioning. That is why a novel pad roughness methodology was developed which is capable of extracting tribological parameters, like the mean asperities radius of curvature and their height and size distribution, from pad roughness measurements. This data was then used for the derivation of the Greenwood-Williamson (GW) CMP model for density and pitch (figures 3 and 4) dependencies in ILD- and STI-CMP processes. It is based on the consideration of the contact mechanics between a patterned wafer and a rough polishing pad and can be applied on both chip and feature level. The GW model provides evidence that pad-roughness is essential to understand planarization and due to the continuously shrinking modern ICs the size effects in CMP will soon become as significant as the density ones.

The transformation of the company structures in the chip production like foundry business with its short time to market and product lifetime of chip generations needs well synchronized processes and design. Therefore, a CMP-suitable design becomes more and more crucial to be capable of competing on the market. Novel CMP modeling approaches are a powerful tool for achieving this goal by enabling new integration paths, more precise design rules and cost effective process development.



3 *Comparison of experimentally measured step planarization (symbols) to GW model predictions for the density and pitch field.*



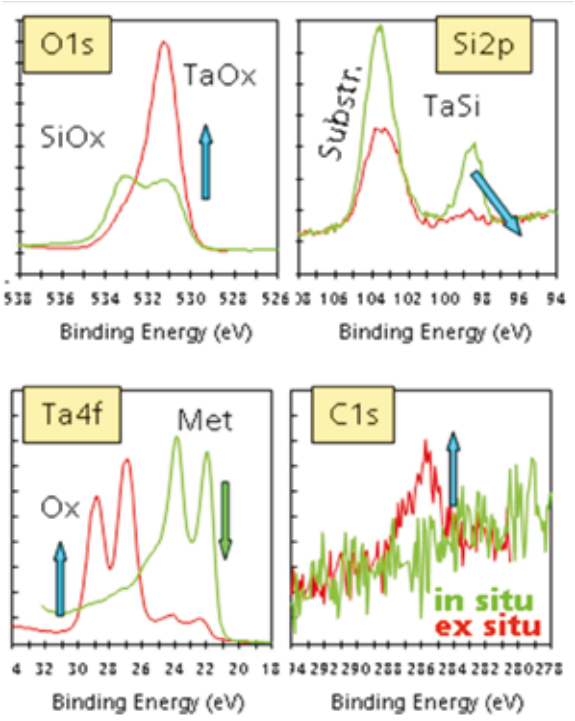
4 *(a) Measured (symbols) and modeled planarization of test structures with 20 µm line width, 20 µm space width and 50 % density.*
(b) Measured (symbols) and modeled planarization of test structures with 50 µm line width, 20 µm space width and 71.4 % density.

FUNCTIONAL ELECTRONIC MATERIALS - BACK END OF LINE

SPECIFIC ANALYTICS

In-situ XPS for inline barrier characterization

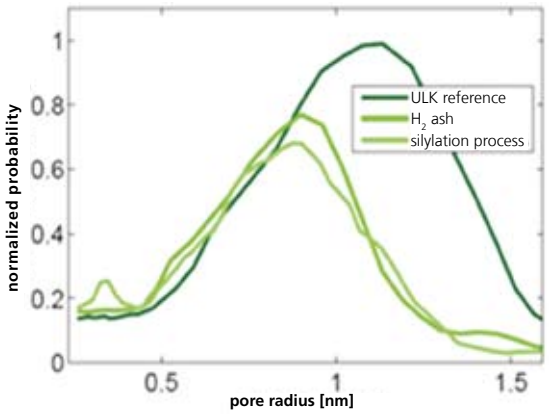
Barriers as the thinnest films in the back end of line are very prone to oxygen. Especially the PVD deposited tantalum nitride/tantalum barriers are oxidizing within minutes. Therefore, we coupled a 300 mm capable XPS with a commercial available barrier/seed cluster tool. As shown in figure 1, there is a significant difference between in-situ and ex-situ measured spectra. Not only changed the tantalum into tantalum pentoxide, but the interfacial tantalum silicide also and the sample is contaminated with carbon.
At Fraunhofer CNT, an additional dual ampoule plasma enhanced CVD chamber was recently coupled to the cluster to develop new barrier systems. The configuration allows unambiguous chemical in-situ analysis for process optimization.



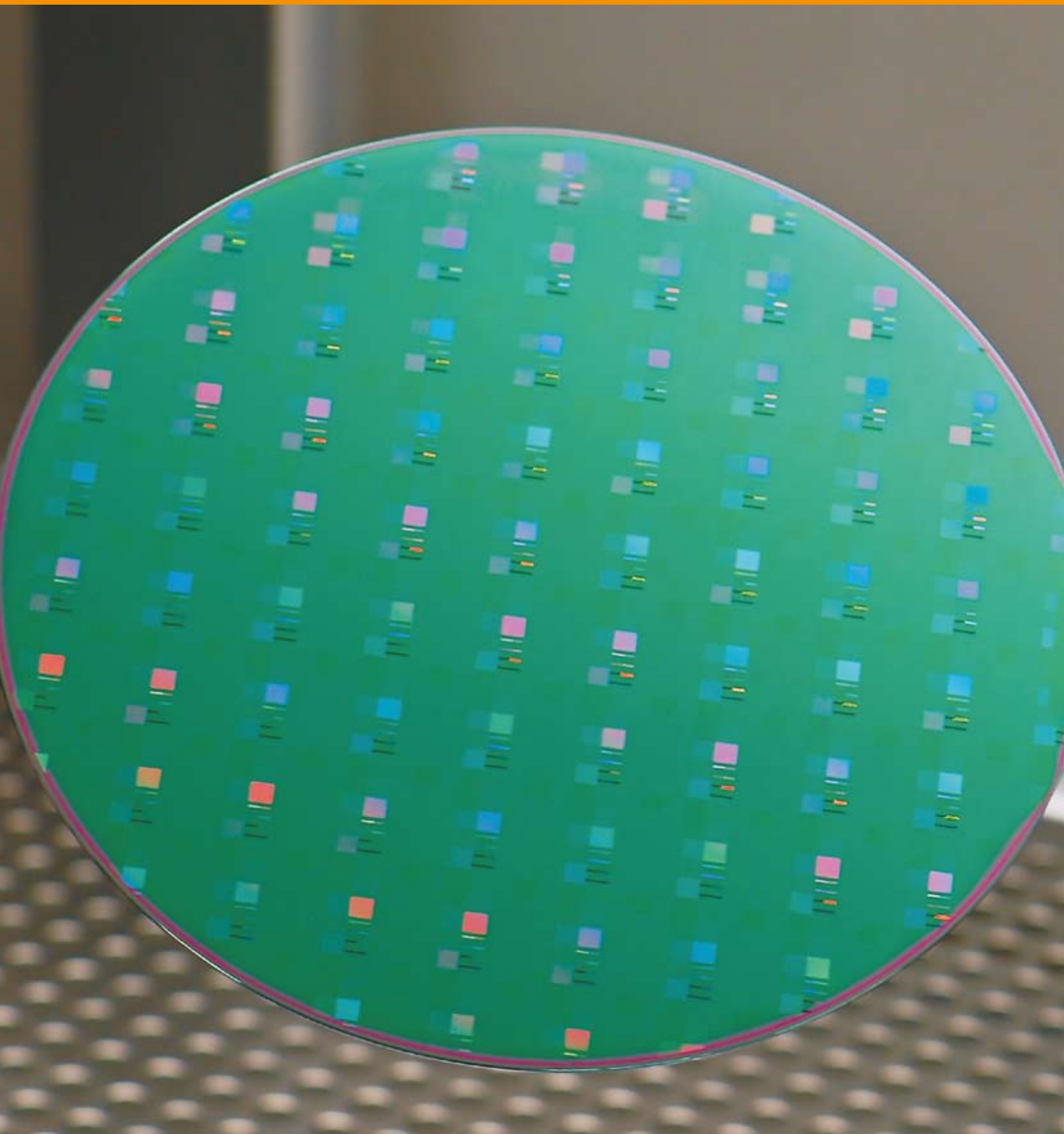
1 *In-situ and ex-situ XPS spectra of tantalum on silicon oxide sample.*

Ellipsometric porosimetry

An ellipsometric porosimeter gives important information about porous dielectric materials. The pore size distribution of an untreated sample was compared to that of a sample after plasma exposure, with and without additional repair treatment (figure 2). It is clearly shown that the plasma process leads to smaller pores, an effect known as densification. Furthermore, it can be seen that the repair treatment results in an additional peak at smaller pore sizes. This can be contributed to the exchange of a bigger functional group at the surface by a smaller one. Apart from the influence of different process steps, other experiments, for example diffusion measurements or barrier integrity studies can be done.



2 *Pore size distribution: Reference, plasma treated and k-restored ULK sample.*



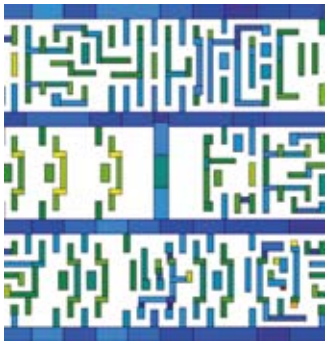
PATTERNING

COMPETENCES

The competence area Patterning provides manufacturing of resist masks in special organic photoresists with patterning sizes down to 35 nm and their transfer into the underlying hard mask. Exposure is carried out using maskless electron beam lithography. The competence area focuses on the preparation of customer and application-specific designs and layouts on 200 mm and 300 mm wafers via a modern and flexible direct patterning process.

TRENDS

In 2010, Fraunhofer CNT's patterning capabilities have been extended to meet customer requirements according to high resolution "More-Moore" applications but also for novel "More-than-Moore" challenges. Research in the field of e-beam patterning has been intensified regarding resist resolution, wafer throughput and overlay as well as most advanced e-beam lithography processes on customer specific substrates and stacks.



1 *Customer layout after e-beam DataPrep.*

2 *E-beam patterning at Fraunhofer CNT: 22 nm node test layout source: GLOBALFOUNDRIES .*

Fraunhofer CNT
Competence Area Patterning

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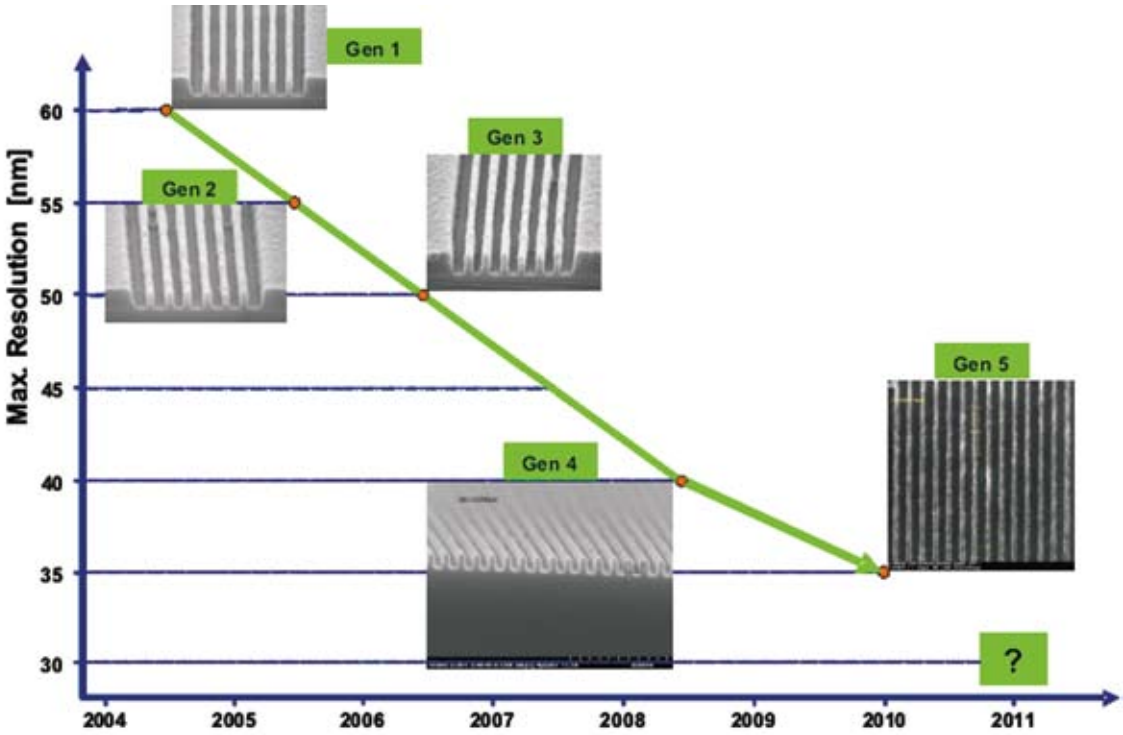
EVALUATION OF NOVEL E-BEAM PATTERNABLE PHOTOMATERIALS

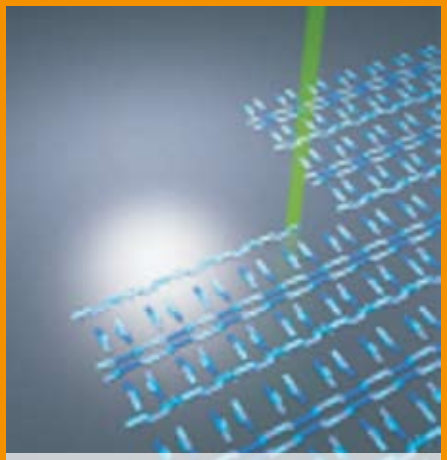
In 2010, significant progress has been generated in the field of resist and materials processing, driven by the race for ever higher resolution requirements according to Moore's law. Today's resolution limit of 50 kV shaped beam systems is seen in the 30 nm CD (critical dimension) regime and large efforts are spent to improve this for the requirements of the 22 nm node. Main contributors for the resolution limitations are the e-beam tool (mainly electron blur impacts), the proximity effect and process related effects dominated by proton diffusion in the resist.

Since 2005, Fraunhofer CNT has established significant know-how in the field of resist and process evaluation and a multitude of materials has been screened on our high-end 300 mm wafer equipment with respect to the requirements of our specific customer needs. Therefore, Fraunhofer CNT is collaborating with most of the leading edge suppliers such as Tokyo Ohka Kogyo (TOK), FujiFilm Electronic Materials and Dow Corning (amongst many others). The performance of these materials such as resolution or line edge roughness has been improved through short learning cycles with the suppliers. Today, resist resolution at Fraunhofer CNT has reached the sub 35 nm regime for lines/spaces as well as for contact holes. Further improvements to cover the needs for the 22 nm lithography node are on its way on the material and process side as well as on the hardware side.



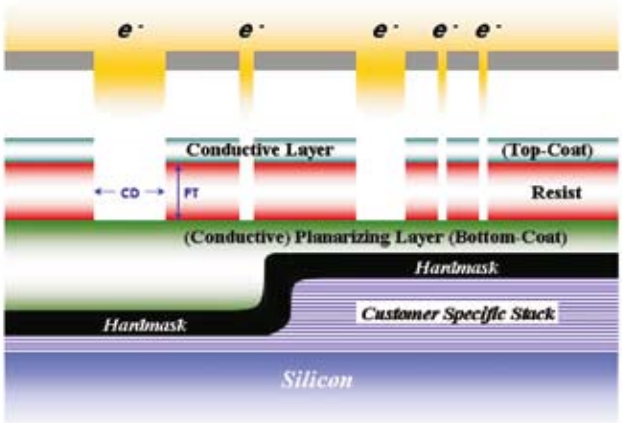
1 *Resolution improvement in positive photoresist (pCAR) since 2005.*

2 *Vistec SB3050DW e-beam direct write tool (50KV Variable Shaped Beam)*



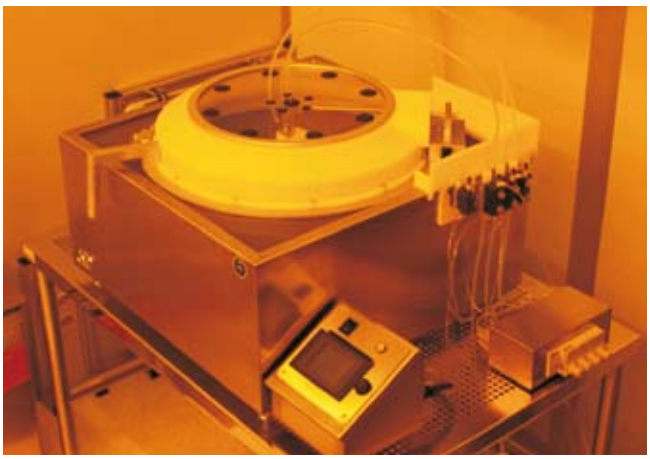
3 *Patterning by e-beam direct write*

Intensive research and development work has been performed at CNT to compensate pattern deteriorating effects such as lack of etch resistance, pattern collapse, 3-D topographical effects, bottom contamination, surface charging or defectivity. Thus, more complex stacks and materials are required today, including customer specific hardmasks, planarizing layers, conductive top and bottom coats (see figure 4).



4 *Scheme of most advanced photomaterial stack.*

In 2010, the existing laboratory equipment for semi-automated coating and thermal cure/baking of photo materials has been extended by the setup of stand-alone processing equipment for consecutive wet development (figure 5). This enables much higher flexibility for non-standard litho material processing on substrate sizes ranging from 4" to 12" wafers and other special substrate types.



5 *Brewer Science Cee® 200FX semi-automated wet developer.*

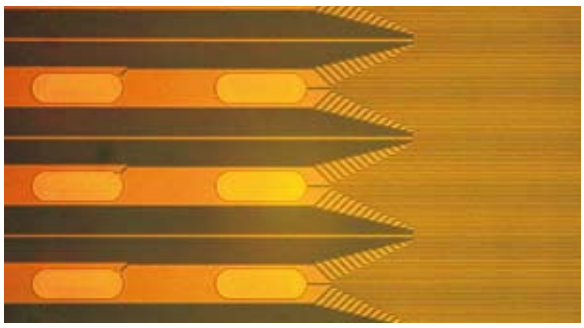
FEASIBILITY STUDY FOR A HOLOGRAPHY DEMONSTRATOR

A new patterning method using electron beam direct write (EBDW) was developed at Fraunhofer CNT for a holography demonstrator for SeeReal Technologies GmbH, Dresden.
The project included data preparation of the customer-specific layout, the development of the complete resist process including coating, baking and developing the wafer, resist patterning using electron beam technology and a final optical inspection. Thus the advantages of EBDW could be fully utilized. Optional design changes could be implemented very fast. Maskless electron beam lithography was the preferred method for this rapid prototyping project for a component of a holographic projection display prototype.

Contrary to other projects, which require high resolution of structures, one of the challenges of this project was to pattern 8 inch glass substrates with a transparent conductive oxide (TCO) (figure 1). New alignment and height mapping concepts for the electron beam were established to overcome difficulties with the transparent stack and substrate. Thereby, the dimension of the smallest TCO electrode was in the lower wave length range of light spectrum. For establishing a proper working resist process stack, compositions were changed and varied facing material delamination and degradation (oxidation). To provide conductivity and to avoid short cuts of the electrodes, high demands in a defect-free process were required.

PATTERNING

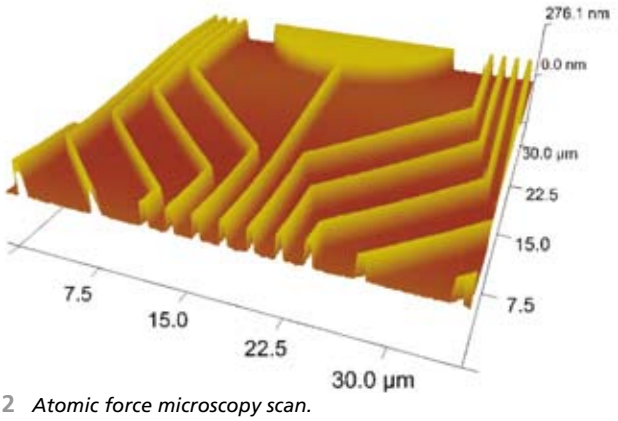
First analyses of appearing defects were done so far and processes were changed and optimized regarding defect density. The etch process for the display component is also very challenging. In general, display components with structures smaller than 1 µm could not be etched with a wet etch process so far. Due to the fact that Fraunhofer CNT is not able to run 8 inch etch processes, the component was etched by another project partner with an RIE dry etch process. The study was realized successfully and a follow up project with SeeReal was agreed upon.



1 *Contact pads and line/space structures.*

Electron beam lithography at a glance:

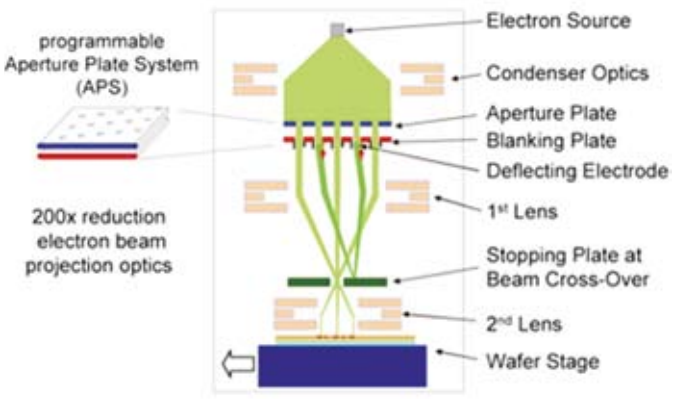
- Litho character: line/space structures
- Critical dimensions: line/spaces: 500 nm/250 nm until 2 µm/2 µm
- Stack: TCO/SiO_2 on 8 inch glass substrate
- Resist: thickness 160 nm, tonality negative, chemically amplified



2 *Atomic force microscopy scan.*

COMPLEMENTARY PATTERNING APPROACH USING MULTI E-BEAM TOOL

Within the EU FP7 program MAGIC, Fraunhofer CNT was involved in the development of maskless lithography (known as "ML2") tools based on multi-beam principles and their integration into CMOS manufacturing. CNT's project partner IMS Nanofabrication developed a high-energy ML2 approach known as PML2 (Projection Maskless Lithography) using up to 250.000 electron beams in parallel (figure 1). In 2010, the last year of the MAGIC project, we demonstrated in collaboration with GLOBALFOUNDRIES and IMS Nanofabrication (Vienna, Austria) a possible future patterning approach for the 22 nm technology node and beyond: "Complementary Patterning".



1 *Principles of projection maskless lithography (PML2).*

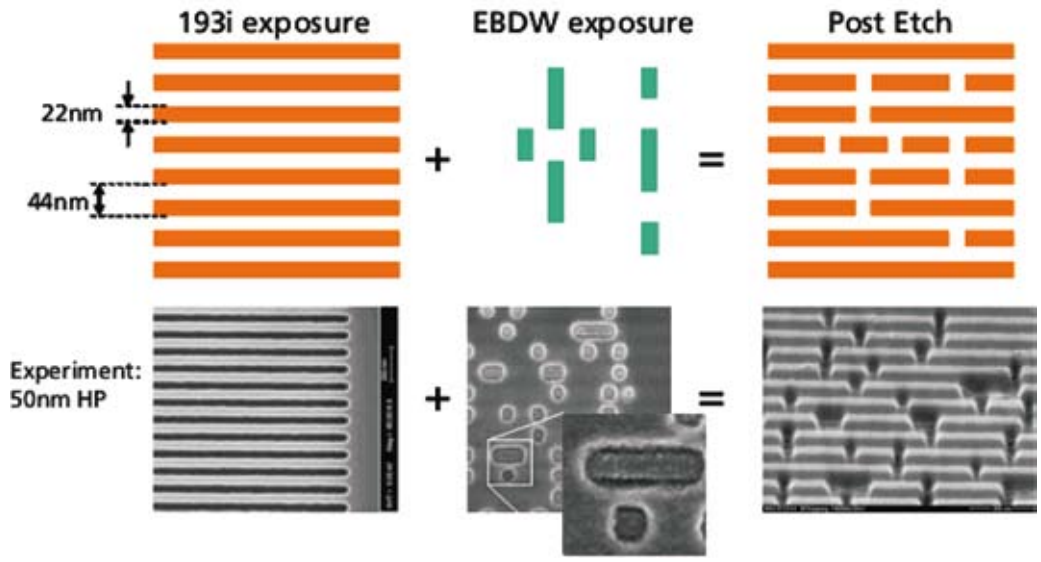
PATTERNING

Yan Borodovsky of Intel was the first who coined this term. He presented a realistic solution of a combination of optical 193 nm immersion/EUV lithography and EBDW at the LithoVision Symposium. Silicon gratings of 50 nm half pitch on 300 mm wafers were provided by GLOBALFOUNDRIES. The resist mask was patterned by optical 193 nm immersion lithography using quadrupole illumination. The resist features were transferred into the silicon bulk via a standard hard mask. The result of this first silicon etch step can be seen in figure 2.

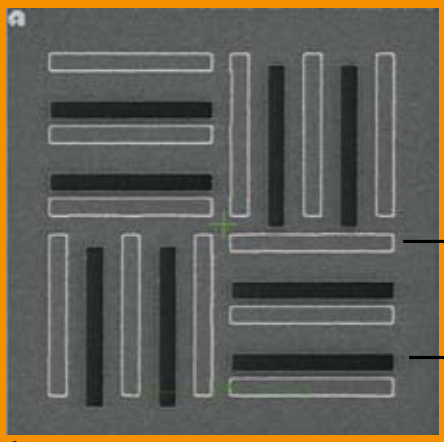
At Fraunhofer CNT the pre-structured wafers were coated using a special HSQ resist process which allows a smooth capping and void-less filling of the silicon grating. HSQ coated 300 mm wafers were sent to IMS Nanofabrication to be exposed using the PML2 Alpha tool. The layout to cut the lines was designed by Fraunhofer CNT.

It basically simulates a realistic SRAM or logic Metal interconnect layer to be cut gaps, vias or contacts into 1-D GDR (one-dimensional gridded design rule) lines. The result of the second Litho step is shown at the right of figure 2.

After e-beam lithography the wafers were cleaned and etched at Fraunhofer CNT using advanced Ar/NF_3 based plasma process in a magnetically enhanced reactive ion etching (MERIE) chamber gaining an etching selectivity HSQ:Si of about 1:10. The cross-sectional view on a small cut hole clearly shows sufficient etching depth. In conclusion, Fraunhofer CNT, GLOBALFOUNDRIES and IMS Nanofabrication successfully demonstrated the feasibility of complementary patterning using 193i lithography and multi-EBDW in a mix-and-match approach.



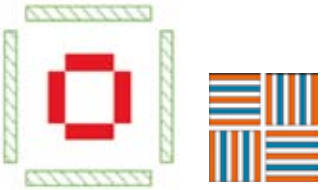
2 *Mix & match approach to combine high throughput (opt. litho) and high resolution/high flexibility (e-beam).*



1 *Fully processed CD-SEM measurement target*

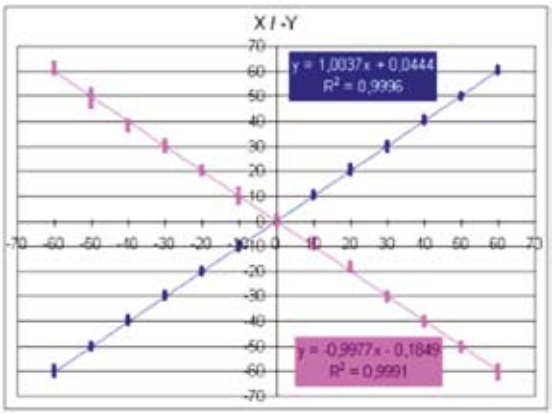
CD-SEM OVERLAY MEASUREMENT USING SMALL HIGH PRECISION TARGETS

The lithography tool park at the Fraunhofer CNT does not feature a stand-alone overlay measurement tool. Within the BRIDGE project, we checked and improved the overlay performance of our exposure tool and measured and corrected the occurring overlay error in a real life application. For this reason, an overlay measurement target and measurement scheme as shown in figure 1 was set up. The target is split up into two layers. The first layer (bright) contains the outside bars and the second layer (dark) the ones on the inside. Opposed to normal BiB targets used in optical lithography (figure 2, drawing to scale), the CD-SEM targets are much smaller (24 x 24 µm² vs. 9.5 x 9.5 µm², figure 2), save 84 % space, use less writing time and improve measurability and accuracy in the CD-SEM measurement. The newly designed target can be further reduced in size for in-chip placement.



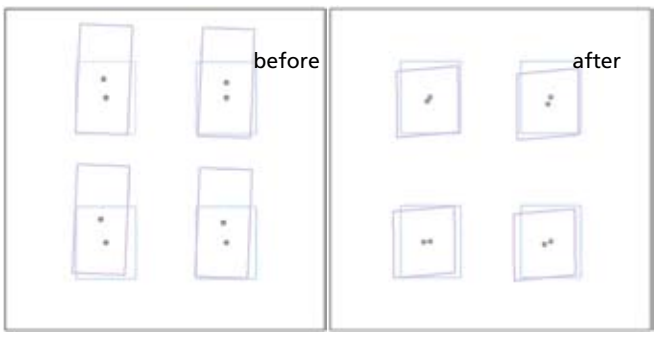
2 *Box-in-Box target (left) versus CD-SEM OVL target (right).*

First studies with a designed overlay translation error in X and Y direction showed that the measurement accuracy is very good and the results yield the expected values (figure 3). The mean measured overlay deviation was smaller than 0.2 nm and the spread of all measured overlay values (3σ) smaller than 3.4 nm. Moreover, the linear fit was almost perfect ($R^2 > 0{,}999$). The last step was the integration of the CD-SEM target in a two-layer test chip layout. After complete processing of layer 1 and finished litho layer 2, the target looks like shown in figure 1. The overlay measurements are taken between the remaining lines where the shift corresponds to the respective overlay error in this location. On every exposure field (test chip) there are at least four measurement locations in order to be able to reconstruct all overlay contributions (translation, magnification, rotation and field specific parameters).



3 *Results of the designed overlay error measurements.*

After evaluation of the measured data points a clear trend was visible. All four field parameters were almost zero and could be omitted in the correction. The other six wafer parameters were calculated and fed back to the tool for the next wafer exposure. As visible in figure 4, the correction applied corrects most of the overlay error. The same procedure can be applied to any prepared layout containing the newly designed CD-SEM overlay targets. The automation of the evaluation process is currently ongoing.



4 *Plots of overlay error before and after correction.*

DEVICES & INTEGRATION

COMPETENCES

The main research topic of the competence group "Device & Integration" is the development and integration of nanoelectronic devices. Furthermore, the main focus is on the electrical characterization of semiconductor devices on wafer level such as memory devices (single memory transistors, arrays and demonstrators) as well as the development of concepts for the integration of new materials and innovative etching processes in process flows in order to fabricate nanoscaled structures. This work is assisted by simulations on device and process level.

TRENDS

With the recent developments in integrating new thin-film materials such as high-k gate dielectrics, many process integration issues have to be solved in order to meet the reliability targets and to benefit from a low power consumption and high-operating frequency of devices in the 2x nm scale. For structuring the new materials, advanced etching processes needs to be developed for achieving good uniformity and low damage of adjacent structures. The etching plays also a big role in the fabrication of deep trenches with small diameter that are used for 3D-capacitors but also for the TSV packaging technology. Here, research is focusing on gaining high aspect ratios while maintaining smooth trench surfaces.

The electrical characterization is addressing the challenges of the new materials and processes. Therefore, advanced reliability characterization methods of high-k materials and the development of new test structures for process monitoring are on the roadmap as well as the investigation of reliable probing and testing on small contact pads that are important to reduce the chip-area and to enable new packaging concepts.

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Devices & Integration

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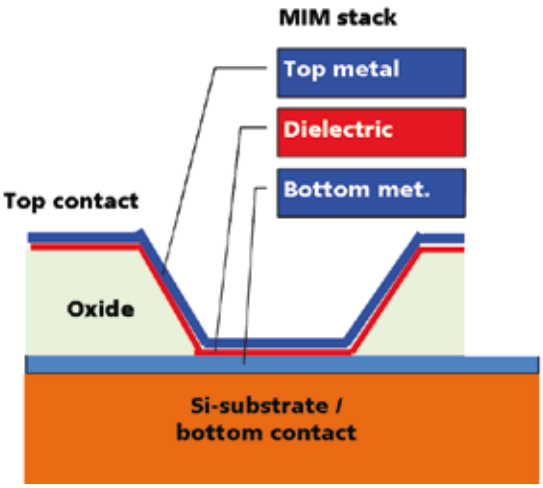
ELECTRICAL ASSESSMENT OF MATERIALS, PROCESSES AND INTEGRATION CONCEPTS

For rapid learning of materials and processes at Fraunhofer CNT, a flexible unit process development platform was set up. Multi-functional testchips were fabricated including MIM/MIS structures for detailed electrical validation of functional nano-layer systems, e. g. high-k process development and qualification. Different unit processes and their research activities are involved to achieve a full process chain for testchip fabrication.

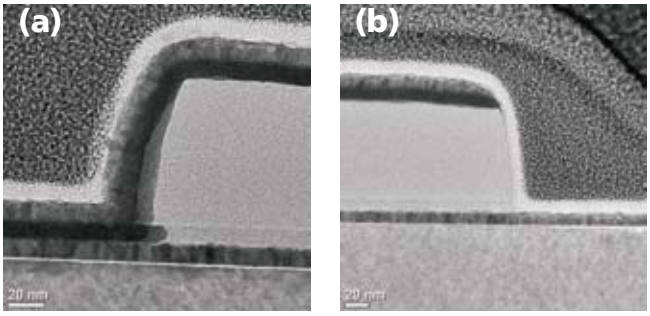
The patterning of nano-layer systems is carried out very flexibly by means of e-beam lithography. For the purpose of the development of next generation patterning processes, dedicated structural e-beam testpattern layouts were established aiming at the enhancement of e-beam tool performance (resolution, improved line-edge roughness) on the one hand and at the research on novel etching methods and chemistries on the other.



1 *Schematic cross section of the MIM structure.*

MIM CAPACITOR INTEGRATION CONCEPT

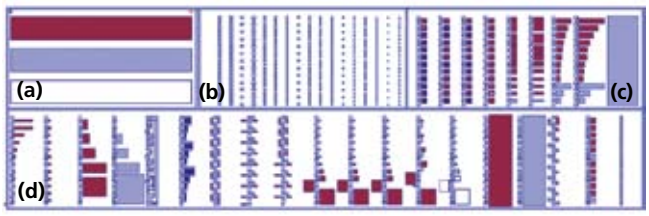
An integration concept was developed to fabricate planar MIM capacitors (shown in figure 1) consisting of two lithography layers - one to open the capacitor areas; a second to pattern the top electrode isolating small capacitor structures from each other. To realize a fully functional development platform, a standard processing chain had to be set up combining a series of processing steps, such as material deposition, cleaning, etching routines and metrology investigations. With small changes this integration concept can also be used to fabricate metal-insulator-silicon (MIS) structures, the main layer stack of a transistor. Both flavors (MIM and MIS) were successfully fabricated showing overall very good electrical performance.



2 *TEM micrographs of (a) MIM taper area and (b) top/bottom electrode separation.*

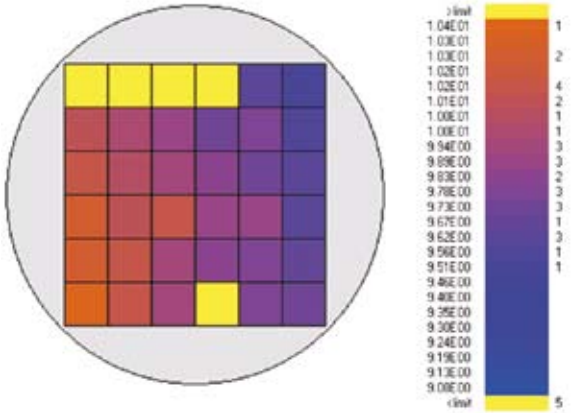
DEVICES & INTEGRATION

A dedicated test chip (figure 3) was designed not only to enable electrical characterization of MIM/MIS structures. It allows also the electrical assessment of various unit processes, the measurement of parasitic components up to critical integration issues. By using standardized contact interfaces, the design considers also the aspects of automated device characterization for measurements on high statistics such as reliability test.



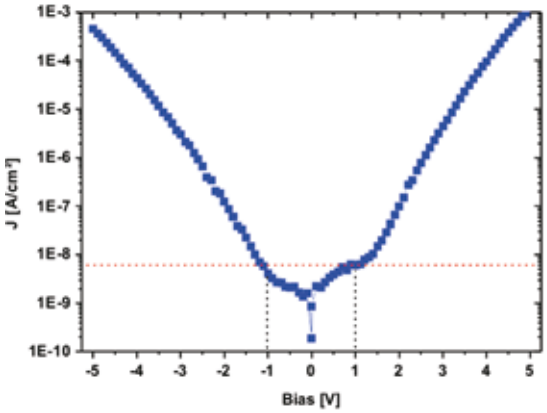
3 *MIM test chip overview with (a) test areas for inline metrology (thickness, sheet-resistance), (b) structures for contact stability test, (c) structures for electrical assessment of high-k etch-damages (d) test structures for general MIM and process characterization.*

As shown in figure 4, wafer mapping of MIM capacitance data can be used to electrically assess the impact of the gas-flow direction during ALD processing. The current-voltage (IV) characteristics in figure 5 show very low leakage behavior of a typical MIM structure.



4 *Electrical thickness map across an entire wafer based on capacitance measurements.*

Based on the experiences gained from the presented research activities, the characterization platform is now available for succeeding projects to assess future integration concepts, materials and processes making them ready for future applications. Advanced research topics such as 3-dimensional (3D) integrated high-k dielectrics based MIM/MIS capacitors are waiting for their evaluation.



5 *IV characteristic of a typical MIM device.*

To demonstrate a potential application, researchers at Fraunhofer CNT developed a self-powered sensor system (see separate article on page 54) whose energy storage element comprises a MIM capacitor with integrated high-k dielectrics.

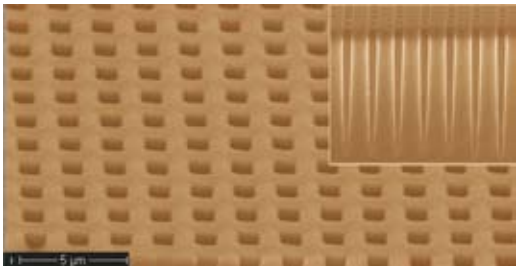
6 *Capacitor chip used as energy storage device.*

DRY ETCH CAPABILITIES - PATTERN FABRICATION, PROCESSES AND PROTOTYPES

The reorientation of Fraunhofer CNT in the last two years results in a diversification of capabilities in many areas. Within this development, the transfer of structures into typical semiconductor materials such as silicon, dielectric materials or even new high-k materials using plasma etch processes has been in a special focus in the year 2010. With the start of the project BRIDGE, Fraunhofer CNT's etch group continuously increased the application possibilities into both directions, materials as well as critical dimensions. The resulting etch process portfolio can be splitted into four categories.

High Aspect Ratio Silicon Etch

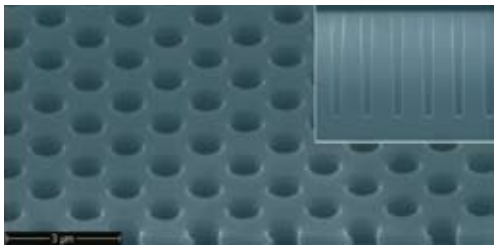
Silicon etching is an essential processing step in semiconductor industry that enables fabrication of products in many application fields such as integrated circuits (ICs) or micro electro mechanical devices (MEMS). These applications often require silicon structures with high aspect ratio to build devices like capacitors, sensors or interconnect vias. The superior etch technology of Fraunhofer CNT enables patterning of silicon trenches and lines with high aspect ratios, smooth sidewalls and low feature size dependency in a wide range of dimensions.



1 *High aspect ratio silicon etch.*

High Aspect Ratio Dielectric Etch

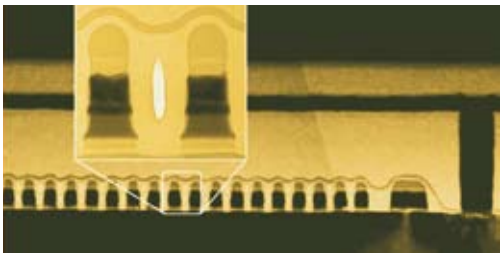
Dielectric materials such as silicon oxide or silicon nitride are typically used as hard mask materials, interlayer dielectrics (ILD) or as matrix material implementing capacitors into integrated circuits. With increasing pattern density, higher aspect ratios are required and the etching of these materials is becoming an important issue. Therefore, the process research at Fraunhofer CNT combines state-of-the-art equipment with in-situ analytics for high flexibility in development.



2 *High aspect ratio dielectric etch.*

Superior High-K Patterning

Plasma etching for sub 45 nm CMOS technology nodes has reached a new complexity with the implementation of new high-k materials based on transition metal oxides. These materials bring many challenges during patterning due to their high etch resistance and low volatile etch products. Etching processes at elevated temperature at Fraunhofer CNT open up the way to achieve structures with well defined dimensions and straight profiles.

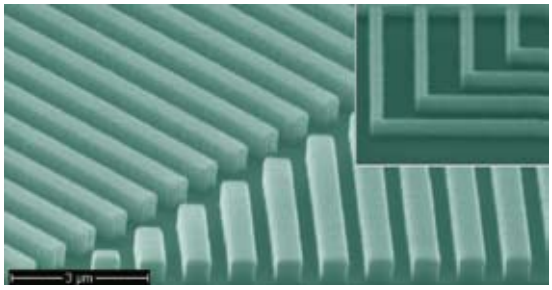


3 *Superior high-k patterning.*

DEVICES & INTEGRATION

Test Pattern Fabrication

Flexible test structures are needed in almost every phase of product or process development, e. g. to characterize fill processes on 3D structures or test functionalities of sensor patterns. Fraunhofer CNT's fast prototyping combines highly flexible maskless e-beam patterning technology and dry etch processing for various materials such as silicon, dielectrics, high-k materials and most metals. We implement customer ideas and enable test pattern fabrication on individual needs.

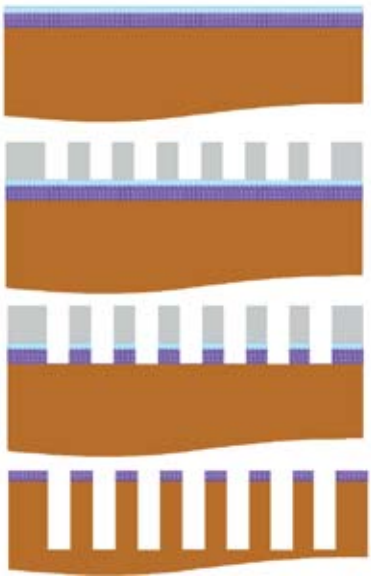


4 *Test pattern fabrication.*

PATTERNING OF DEEP SILICON TRENCHES USING A NOVEL HARD MASK CONCEPT

The fabrication of nanostructured surfaces addresses a broad variety of novel applications in modern nanoelectronics and is one of Fraunhofer CNTs focus topics. Regular pattern are typically formed by exposing a photo resist and pattern transfer by plasma etch processing using hard mask technologies. The fabrication of scaled high aspect ratio trenches (width < 100 nm, aspect ratio > 10) and holes has proven to be a challenge using conventional patterning concepts.

For future technology nodes it becomes even more challenging due to the ongoing lithography trend to reduce the resist thickness as predicted by the ITRS. This is mainly driven by the decreasing depth-of-focus (DOF) in optical lithography that is using projection lenses with higher and higher numerical aperture (NA). Even though NA is more relaxed for EUV lithography, DOF stays small because of the extremely small EUV wavelength. Another driver to reduce resist thickness is the maximum aspect ratio of about 3:1 due to pattern collapse. Therefore, the ITRS predicts resists with a maximum thickness of 100 nm for 32 nm node in 2012.



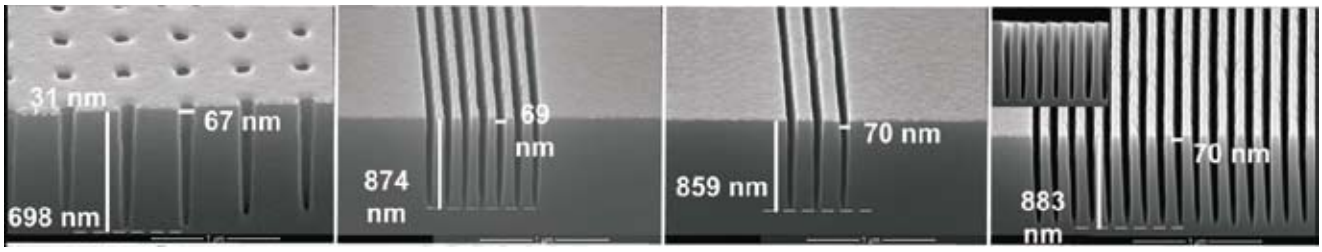
1 *a) Deposition of hardmask stack*
b) Pattern transfer by e-beam lithography
c) Hard mask open etch
d) Pattern transfer into silicon using the novel hard mask material

In disagreement with the lithography trends the pattern transfer is challenged by the reduction of resist thickness. The maximum etch depth achievable is mainly limited by etch selectivity of the mask material. For patterning of common hardmask materials (poly-Si, SiO_2 or Si_3N_4) with thicknesses above 100 nm thicker resists are needed due to the limited selectivity.
As the thickness reduction has been essential to enable high resolution patterning, novel hard mask technologies with reduced layer thickness and improved selectivity to the functional layer are required.

Fraunhofer CNT has developed a concept using a thin resist in combination with novel hard mask layers to pattern trenches and holes deeper than 500 nm into the silicon wafer using conventional semiconductor processes. The implementation of a thin hard mask provides the opportunity to use thin resist layers for the patterning with relaxing etch process requirements (i. e. selectivity). The novel hard mask stack consists of materials which are fully compatible with standard semiconductor fabrication.

For a successful integration of the novel hard mask technology, the development of the hard mask open process was essential. A CCP type plasma etch chamber (part of Fraunhofer CNT's plasma etch tool set) was used to provide a well defined and steep sidewall angle which is essential for an excellent transfer of the structure into the target material.

The standard silicon etch process was used to create trenches and holes simultaneously with etch rates in a range between 1 to 2 µm/min. Small trenches and holes of 70 nm in width and ~600 nm in depth were prepared. During etch processing the consumption of the hard mask layer is very low and the achievable etch selectivity was >100:1 for the new hard mask material (figure 2).



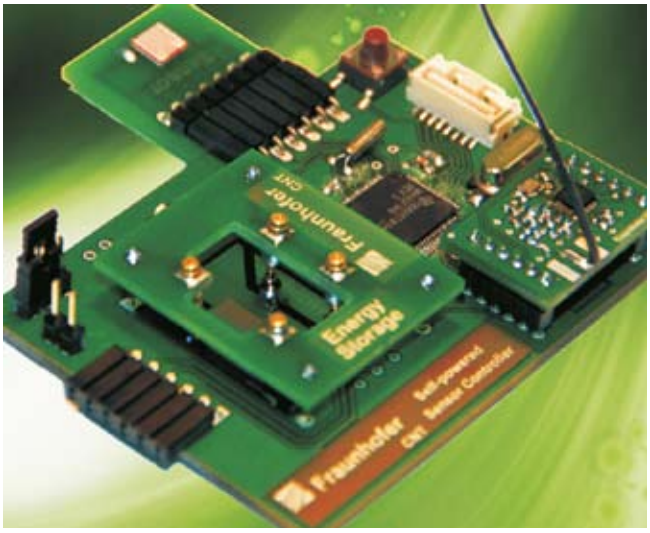
2 *Deep silicon trenches etched via novel hard mask material, consumption of hard mask layer is less than 5 nm.*

DEVICES & INTEGRATION

HIGH DENSITY NANO-CAPACITORS FOR SELF-POWERED SENSOR SYSTEMS

Self-powered sensors can be widely used in many applications where wiring and batteries are inappropriate. Powered by solar cells or thermoelectric generators the sensors can acquire and distribute telemetry data in buildings or agriculture.

Even in industrial facilities and many places with limited accessibility the maintenance-free sensors are able to monitor processes over long periods. In order to operate the sensors at limited availability of energy sources, an elaborate power management, low power devices and internal energy storage are required.



1 *Demonstrator system developed by Fraunhofer CNT.*

With its competences in projection and design of self-powered wireless sensor systems including power management and internet access to the sensors, Fraunhofer CNT offers customized development services to companies that want to employ sensor systems in their applications.

Meeting the requirements of limited space for tiny sensors, Fraunhofer CNT develops high density on-chip energy storages that can be integrated together with the other components of the system on a single chip. The integrated energy storage is enabling new applications that require very small and thin sensor systems, needed for health monitoring, in pipelines or moving parts of engines. Fraunhofer CNT is working on new dielectric materials and patterning processes in order to provide high energy storage capacitances using CMOS compatible technologies.

Application

Si-based high density capacitors for various applications:

- Integrated energy storage for self-powered sensor systems
- Decoupling capacitors for SoC solutions
- Power supply filters

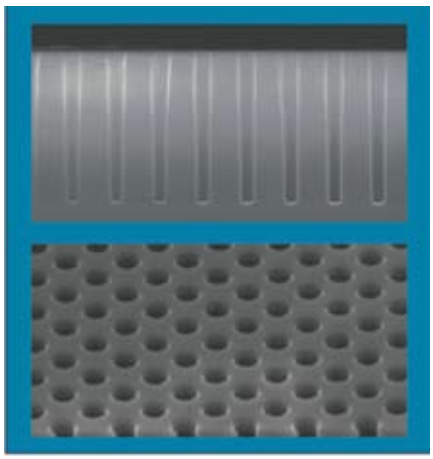
Capacitor specification

- Target: 500 nF/mm², up to 5V
- Long-term development objective: 1 µF/mm²

2 *Capacitor chip used as energy storage device.*

Technology for high capacitance density

- Large area gain by three-dimensional (3D) integrated capacitor trenches
- Special high aspect ratio reactive ion etch (RIE) process technology enables high surface area gain
- High-k dielectric material deposition using ALD processing 300 mm silicon wafer processing
- Compatibility with standard and leading edge CMOS technology



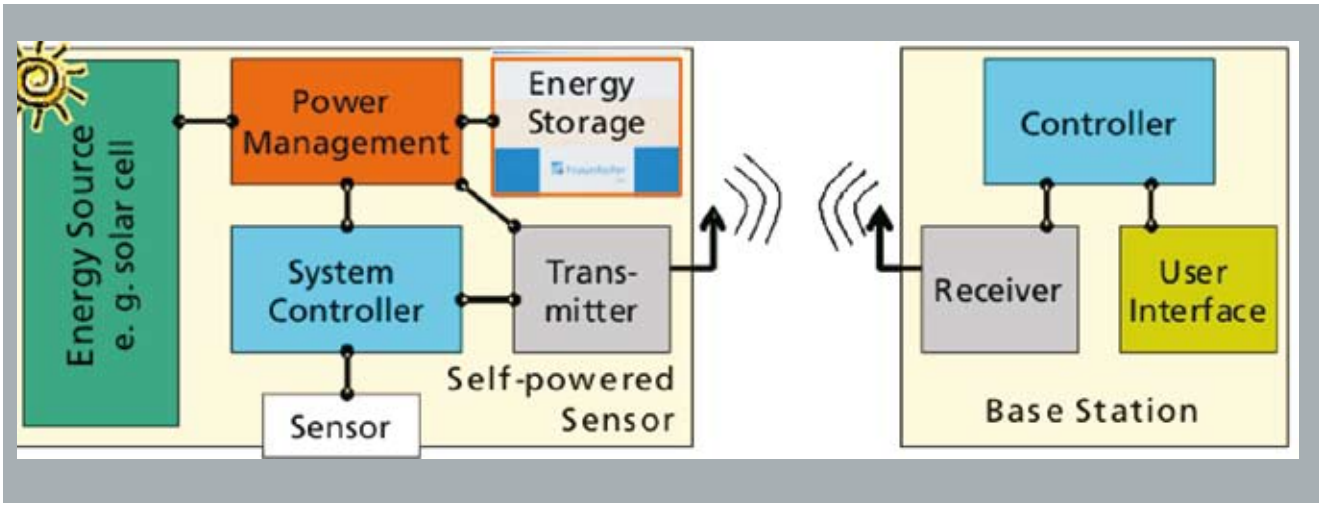
3 *SEM cross-section and top-down images of the integrated three-dimensional trenches (enlarging the capacitance area).*

Features

- Demonstration of wireless sensor network with multiple sensors
- Can be also used as data logger for applications with limited wireless access (e. g. monitoring of goods)
- Low power system design
- Power management uses integrated energy storage as energy buffer
- Energy monitoring and adaptive system operation
- Base station equipped with webserver for sensor access via internet

How it works

- Energy harvester has limited output power
- Harvested energy is therefore buffered on energy storage capacitor
- System activity only in small time slots
- Current for system activity and wireless data transmission (~15mA) sourced by energy storage device
- Ultra-low power consumption during sleep phase (< 1µA)
- System controller processes sensor data, monitors available power and controls system activity

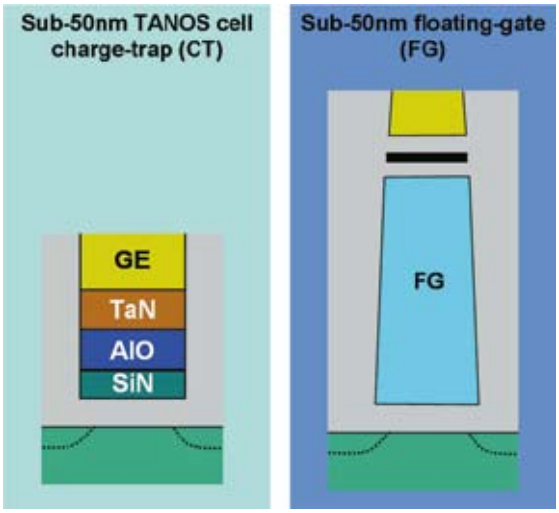


4 *Functional block diagram of demonstrator system.*

DEVICES & INTEGRATION

MEMORY RELIABILITY - RANDOM TELEGRAPH NOISE (RTN)

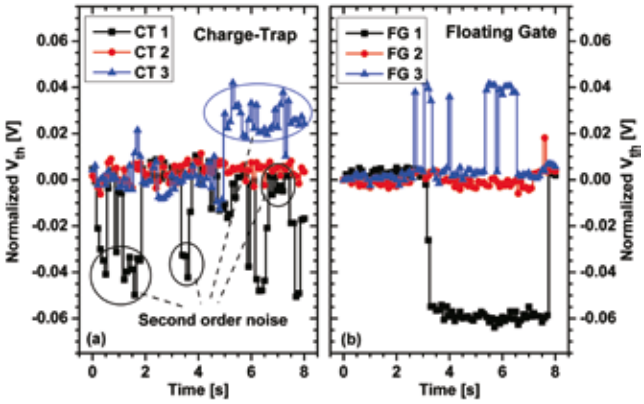
The Random Telegraph Noise (RTN) effect is one of the reliability issues for memory technologies, like SRAM and NAND Flash, but also for small logic transistors in the deca-nanometer scale. The RTN effect is a randomly occurring discrete variation of the drain current and can also be translated into a discrete variation of the threshold voltage (Vth). As a consequence, due to shifted Vth a false detection of logic state could occur and may cause logic malfunction or single bit failures when reading memories.



1 *Schematic cross section of TANOS (left) and floating gate (right) cell.*

The discrete variation is induced by interface traps in the gate oxide/channel interface region that are capturing and emitting charges. As a consequence, charge variations of single electrons close to the channel can cause significant Vth changes in the 100 mV region. Unlike the impact of extrinsic defects, an RTN event can affect every transistor due to the relationship to intrinsic interface trap density. The RTN effect is amplified mainly when shrinking the transistor size or when using thicker gate oxides (>5 nm) that are required for NAND memory cells. The leverage of single electron capture and emission events increases in both cases.

In the frame of the EU-project GOSSAMER, Fraunhofer CNT investigated the RTN behavior of charge-trap-based (CT) TANOS memory cells and compared the results to conventional floating gate (FG) memory cells (figure 1). Except for the gate-stack, both sub-50 nm memory technologies were fabricated similarly using the same test chip layout. Comparing the Vth fluctuation of selected memory cells (figure 2), both memory technologies reveal a similar magnitude of RTN behavior.

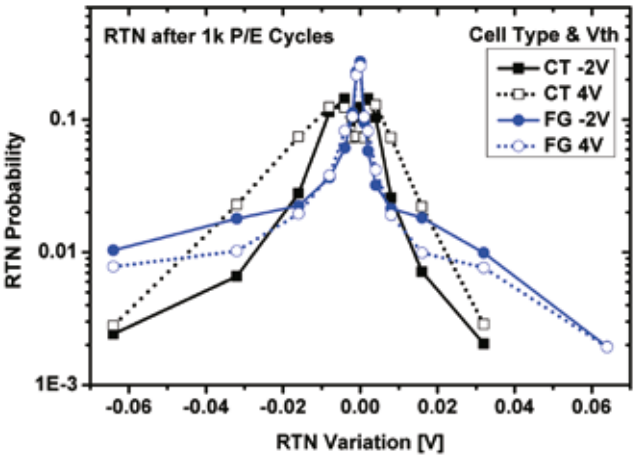


2 *Vth raw data of typical (a) CT TANOS cells and (b) FG cells over time.*

However, for CT cells a superimposed second order noise (SON) was observed being not prominent on FG cells.
A direct quantitative comparison can only be done when using statistical approaches. Therefore, the scientists at Fraunhofer CNT developed new statistical characterization methods in order to estimate the reliability impact of RTN on product level based on single cell characterization results.
The result comparing the probability of RTN amplitudes for CT and FG cells is shown in figure 3. It can be seen that RTN behavior of CT cells is more dependent on cell Vth compared to FG cells.

This effect is related to a difference in stored charge mobility of CT and FG technologies. Secondly, the SON can be clearly identified only on CT cells. It is assumed that the SON is a thermally activated noise in the CT storage layer or its interfaces. Research on this effect is ongoing.

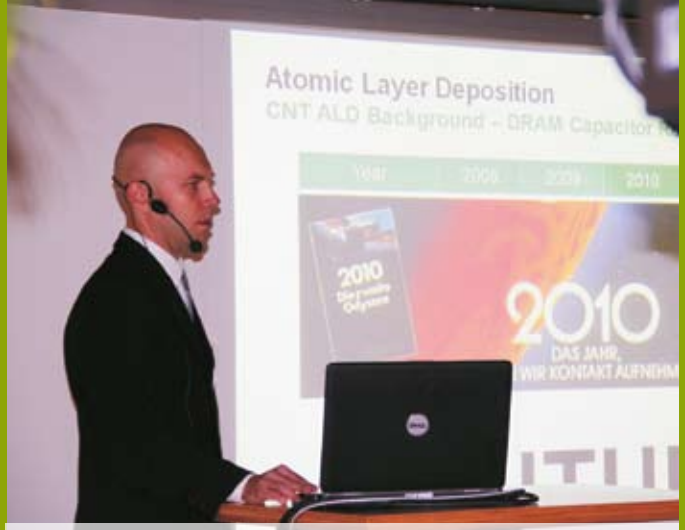
This work has been partly supported by the European Commission under the FP7 research contract 214431 „GOSSAMER" and was presented at the IEEE INTERNATIONAL INTEGRATED RELIABILITY WORKSHOP (IRW) 2010 in Lake Tahoe, CA.



3 *Vth probability of Vth variation comparing programmed (4V) and erased (-2V) CT cells with FG cells. FG cells show lower impact of Vth variation and also higher probability for higher RTN magnitudes as compared to CT cells.*

EVENTS

Fraunhofer CNT Research Day in October 2010



Dr. Jonas Sundqvist in the TechArena at the Semicon Europe 2010

Dr. Ahmed Shariq at the Analytica 2010 in Munich

FRAUNHOFER CNT TRADE FAIR ACTIVITIES IN 2010

March 2010	
Analytica, International Trade Fair for Laboratory Technology, Analysis and Biotechnology	Munich, Germany
May 2010	
Silicon Saxony Day	Dresden, Germany
July 2010	
nanofair, International Nanotechnology Symposium	Dresden, Germany
October 2010	
SEMICON Europe 2010	Dresden, Germany
November 2010	
Electronica 2010, Components, Systems, Applications	Munich, Germany

Das Fraunhofer CNT präsentierte sich 2010 auf insgesamt fünf Messen und Ausstellungen mit neuesten Entwicklungen. Das Institut nahm erstmalig an den Messen Analytica und der Electronica teil und präsentierte sich auf dem Fraunhofer-Gemeinschaftsstand.
Besonders gefragt waren die Analytikleistungen des Fraunhofer CNT, vor allem die Atomsondentomographie sowie das energieautarke Sensorsystem.

In 2010, Fraunhofer CNT presented its latest research results on five tradeshows and exhibitions. For the first time the institute participated in the Analytica and the Electronica at a shared exhibition booth together with other Fraunhofer institutes.
The analytic services, like the atom probe tomography as well as the self-powered sensor system, were especially popular among the visitors.

EVENTS

FRAUNHOFER CNT RESEARCH DAY 2010

Am 28. Oktober fand der erste Fraunhofer CNT Research Day statt. Spannende Vorträge von externen Experten und Wissenschaftlern des Fraunhofer CNT standen im Mittelpunkt dieses Tages. Es konnten hochkarätige Referenten von GLOBALFOUNDRIES, IBM, ASM und weiteren bekannten Unternehmen der Mikroelektronik gewonnen werden. Neben den externen Vorträgen wurden Ergebnisse aktueller Forschungsarbeiten von Wissenschaftlern des Fraunhofer CNT vorgestellt.
Knapp 100 nationale und internationale Gäste aus Politik, Wirtschaft und Wissenschaft kündigten ihre Teilnahme an. Die zahlreiche Teilnahme und das positive Feedback der Gäste lässt uns auf eine gelungene Veranstaltung zurückblicken.
Zukünftig soll der Research Day als feste jährliche Veranstaltungsreihe am Fraunhofer CNT etabliert werden.

The first CNT Research Day took place on 28th October 2010. Recognized experts of leading companies in the microelectronics business, such as GLOBALFOUNDRIES, IMB and ASM, as well as scientific staff representatives of Fraunhofer CNT gave exciting talks on their latest research results and innovations.

Almost 100 national and international guests from politics, industry and science took part in the event. The large number of participants and the positive feedback show the success of the Research Day. Thus, it will become a regular event at the Fraunhofer CNT.

LANGE NACHT DER WISSENSCHAFTEN

Am 18. Juni 2010 fand die 8. Dresdner Lange Nacht der Wissenschaften statt. Das Fraunhofer CNT präsentierte sich im Fraunhofer Institutszentrum auf der Winterbergstraße. Die Besucher des Standes konnten an einem Modell den Weg vom Sand zum Superchip verfolgen oder an einer Animation eine Reise in die Nanowelt antreten. Zusätzlich gab es die Möglichkeit, einen Chip unter einem Mikroskop unter die Lupe zu nehmen, sich in einem Reinraumanzug fotografieren zu lassen sowie sein Wissen in einem Quiz zu testen.

NIGHT OF SCIENCES

The 8th Night of Sciences took place on 18th June 2010. Fraunhofer CNT participated with a booth at the Fraunhofer institute center at Winterbergstraße. Visitors could follow the way „from sand to superchip" on a model. They could experience a jouney into the world of nanoelectronics. They had the chance to examine microchips with a microscope or to slip in clean room clothes and to test their knowledge by participating in a quiz.

FRIDAY@FRAUNHOFER

Am 1. November 2010 besuchten Schüler der 12. Klasse des Grundkurses Biotechnologie/Bionik des Marie-Curie-Gymnasiums anlässlich des Friday@Fraunhofer das Fraunhofer CNT, um an einem Vortrag sowie einer Window- und Labortour teilzunehmen. Bei einem Besuch des Reinraums konnten die Schüler eine Menge über die Forschung, z. B. im Bereich der Halbleiter, deren integrierte Schaltkreise mit Strukturbreiten unter 100 nm, die Charakterisierung von Materialien oder innovative Analyse- und Prozessmethoden lernen.

FRIDAY@FRAUNHOFER

Pupils of the secondary school Marie-Curie-Gymnasium, with basic courses in biotechnology/bionics, visited Fraunhofer CNT on the 1st November 2010 to listen to a lecture and to take part in a window and laboratory tour. During a visit in the clean room, students learned a lot about research, they got information about semiconductors, integrated circuits with dimensions below 100 nm, material characterization or innovative analytical and process methods.

WISSENSCHAFT TRIFFT INDUSTRIE

Am 1. Juli 2010 begrüßte das Fraunhofer CNT Vertreter des Industrie-/Technologiekreises des Bundesverbandes mittelständischer Wirtschaft Dresden (BVMW).

In Kooperation mit dem Fraunhofer IPMS bot sich die Möglichkeit eines regen Erfahrungsaustausches sowie Gespräche zu Anknüpfungspunkten für eine potentielle Zusammenarbeit. Im Rahmen der Besichtigung beider Fraunhofer-Institutem konnten die BVMW-Mitglieder einen Einblick in unsere Forschungsarbeit gewinnen.

SCIENCE MEETS INDUSTRY

On 1st July 2010 Fraunhofer CNT had the pleasure to welcome representatives of the "Bundesverband mittelständischer Wirtschaft Dresden" (BVMW).

In cooperation with Fraunhofer IPMS, the participants had the possibility to discuss potential collaboration topics and to gain an insight into the research work at both Fraunhofer institutes in the course of a lab and clean room tour.

EVENTS

COLLOQUIA AT FRAUNHOFER CNT

21.01.2010
40th Fraunhofer CNT Colloquium
Dr. rer. nat. Thomas Schroeder, IHP GmbH
"More than Moore" approaches at IHP to further functionalize SiGe:C BiCMOS technologies

04.03.2010
41st Fraunhofer CNT Colloquium
E. – Bernhard Kley, Friedrich-Schiller University Jena
Subwellenlängenstrukturen in der Optik; Funktion, Herstellung und Anwendung

11.03.2010
42th Fraunhofer CNT Colloquium
Dr. H. Ehrenberg, Leibniz Institute for Solid State and Materials Research Dresden
Elektrodenmaterialien für Lithium-Ionenbatterien: Materialwissenschaftliche Herausforderungen und Perspektiven

20.05.2010
43th Fraunhofer CNT Colloquium
Laurent Pain, CEA-LETI – Nanotec Department
The potential of electron beam lithography

17.06.2010
44th Fraunhofer CNT Colloquium
Dipl.-Ing. Denis Reso, Otto-von-Guericke University Magdeburg
Die Metallorganische Chemie Gasphasenabscheidung (MOCVD) von Germanium-Antimon-Tellurid-Dünnschichten.

02.09.2010
45th Fraunhofer CNT Colloquium
Prof. Dieter P. Kern, University Tübingen, Institute of Applied Physics
Elektronenstrahl-basierte Nanostrukturierung - Materialien und Anwendungen.

30.09.2010
46th Fraunhofer CNT Colloquium
Prof. Minoru Toriumi, Director of „Laboratory for Interdisciplinary Science and Technology", Tokyo
Resist fundamentals in microlithography: Exposure energy loss and dissolution behavior.

18.10.2010
47th Fraunhofer CNT Colloquium
Dr. Jeffrey Gambino, IBM, USA
Improved reliability of copper interconnects using alloying.

PUBLICATIONS

PROMOTIONEN

Im Jahr 2010 konnten wir zwei unserer Mitarbeiter zu ihrer Promotion beglückwünschen, Frau Dr. Katja Steidel und Herrn Dr. Benjamin Uhlig.

Herr Dr. Uhlig verteidigte bereits am 01. Juli 2010 seine Dissertation. In seiner Doktorarbeit befasste er sich mit dem Thema „High Precision Stress Measurements in Semiconductor Structures by Raman Microscopy".
Er arbeitet als Wissenschaftler im Bereich „Functional Electronic Materials - Back End of Line".

Frau Dr. Steidel verteidigte am 02. September 2010 erfolgreich Ihre Dissertation mit dem Titel „Untersuchung der Auflösungsgrenzen eines Variablen Formstrahlelektronenschreibers mit Hilfe chemisch verstärkter und nicht verstärkter Negativlacke." Frau Dr. Katja Steidel ist am Fraunhofer CNT als Wissenschaftlerin im Kompetenzbereich „Patterning" beschäftigt.

DOCTORATES

We were delighted to congratulate two of our colleagues on their doctor's degree in 2010: Mrs Katja Steidel and Mr Benjamin Uhlig.

On 1st July 2010, Mr Uhlig defended his dissertation entitled "High Precision Stress Measurements in Semiconductor Structures by Raman Microscopy". He is a scientist in the competence area "Functional Electronic Material – Back End of Line" at Fraunhofer CNT.

On 2nd September 2010, Mrs Steidel successfully defended her dissertation entitled "Untersuchung der Auflösungsgrenzen eines variablen Formstrahlelektronenschreibers mit Hilfe chemisch verstärkter und nicht verstärkter Negativlacke". She is working as a research associate in the competence area „Patterning" at Fraunhofer CNT.

1 *Dr. Katja Steidel*

2 *Dr. Benjamin Uhlig*

PUBLICATIONS (SELECTION)

INVENTION DISCLOSURES

In 2010, scientists of Fraunhofer CNT were involved in different publications and invention disclosures. On the following pages you will find a selection.

Choi, K.-H.; Gutsch, M.; Freitag, M.; Keil, K.; Jaschinsky, P.; Hohle, C.:
Conventional and reversed image printing in electron beam direct write lithography with proximity effect corrections based on dose and shape modification
(Advanced Lithography Conference <2, 2010, San Jose>) In: Herr, D.J.C.: Alternative lithographic technologies II: 23 - 25 February 2010, San Jose, California, United States. Bellingham, WA: SPIE, 2010. (SPIE Proceedings 7637), 76370W/1-76370W/7

Flachowsky, S.; Illgen, R.; Herrmann, T.; Klix, W.; Stenzel, R.; Ostermay, I.; Naumann, A.; Wei, A.; Hontschel, J.; Horstmann, M.:
Detailed simulation study of embedded SiGe and Si:C source/drain stressors in nanoscaled silicon on insulator metal oxide semiconductor field effect transistors
(International Workshop on Insight in Semiconductor Device Fabrication, Metrology, and Modeling (INSIGHT) <2, 2009, Napa>) In: Journal of vacuum science and technology B. Microelectronics and nanometer structures, Vol.28 (2010), No.1, pp.C1G12-C1G17

Gault, B.; Müller, M.; La Fontaine, A.; Moody, M.P.; Shariq, A.; Cerezo, A.; Ringer, S.P.; Smith, G.D.W.:
Influence of surface migration on the spatial resolution of pulsed laser atom probe tomography
In: Journal of applied physics, Vol.108 (2010), No. 4, Art. 044904, 6 pp.

Jegert, G.; Kersch, A.; Weinreich, W.; Schröder, U.; Lugli, P.:
Modeling of leakage currents in high-k dielectrics: Three-dimensional approach via kinetic Monte Carlo
In: Applied Physics Letters, Vol.96 (2010), No.6, Art. 062113, 3 pp.

Kelwing, T.; Naumann, A.; Trentzsch, M.; Trui, B.; Herrmann, L.; Mutas, S.; Graetsch, F.; Carter, R.; Stephan, R.; Kücher, P.; Hansch, W.:
Comparison of MOCVD- and ALD-deposited $ hbox {HfZrO} {4} gate dielectrics for 32-nm high-performance logic SOI CMOS technologies In: IEEE Electron Device Letters, Vol.31 (2010), No. 10, pp.1149-1151

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Formation of an interface layer between $Al_{1-x}Si_xO_y$ thin films and the Si substrate during rapid thermal annealing
In: Physica status solidi. C, Current topics in solid state physics. Weinheim: Wiley-VCH, 2010, pp. 284-287

Mutas, S.; Klein, C.; Gerstl, S.:
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(MRS Fall Meeting <2009, Boston>) In: Ye, P.D. et al.: High-k Dielectrics on Semiconductors with High Carrier Mobility. Online Proceedings. (MRS Proceedings 1194E), 1194-A04-04

Neuner, J.; Zienert, I.; Peeva, A.; Preusse, A.; Kücher, P.; Bartha, J.W.:
Microstructure in copper interconnects - Influence of plating additive concentration
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Enhancing epitaxial Si_xC_{1-x} deposition by adding Ge
In: Thin solid films, Vol.518 (2010), No. 10, pp.2834-2838

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Investigation of physical and chemical property changes of ultra low-kappa SiOCH in aspect of cleaning and chemical repair processes
(European Workshop on Materials for Advanced Metallization <18,2009>)
In: Microelectronic engineering, Vol.87 (2010), No. 3, pp.457-461

Oszinda, T.; Schaller, M.; Schulz, S.E.:
Chemical Repair of plasma damaged porous ultra low-k SiOCH film using a vapor phase process
(Electrochemical Society (ECS Meeting) <216, 2009, Vienna>) In: Flake, J. et al.: Processing, Materials, and Integration of Damascene and 3D Interconnects: 216th ECS Meeting. October 4 - October 9, 2009 , Vienna, Austria. (ECS transactions Vol.25, Issue 38), pp. 19-30

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